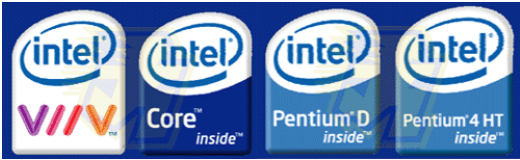


MS-7356 Ver : 0B

Intel (R) LGA775 Processor
Intel (R) Bearlake (GMCH) + ICH9/ICH9R Chipset



- CPU:**
- Intel - Conroe 2.66G (E6700)
 - Intel - Presler 3.73G (PentiumEE965)
 - Intel - SmithField 3.2G (Pentium EE840)
 - Intel - Kentsfield
 - Intel - Prescott 3.73G (P4-EE-3.73GHz)
 - Intel - CedarMill 3.73G (Celeron D356)
 - Intel - Gallatin 3.46G (P4-EE-3.46GHz)
 - Intel - Yorkfield

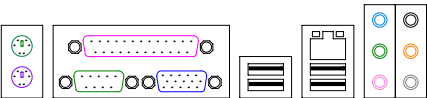
- System Chipset:**
- Intel Bearlake P35/G33 (North Bridge) Rev : A1
 - Intel ICH9 / ICH9R (South Bridge) Rev : A1

- On Board Chipset:**
- CLOCK : ICS9LPRS906BG
 - LAN : RTL8111B
 - IEEE1394a : VT6308
 - IDE Bridge : Marvel 88SE6111
 - LPC Super I/O : F71882FG
 - Audio Codec : ALC888 7.1 Channel Ver : A1
 - BIOS : SPI- 8M

- Main Memory:**
- Dual-channel DDR III * 4 (Max 4GB)

- Expansion Slots:**
- PCI EXPRESS X16 SLOT * 1
 - PCI EXPRESS X4 SLOT * 1 Alternative
 - PCI EXPRESS X2 SLOT * 2 Alternative
 - PCI 2.2 SLOT * 2

ATX Size 305mm * 244mm(OSP)

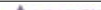


RoHS

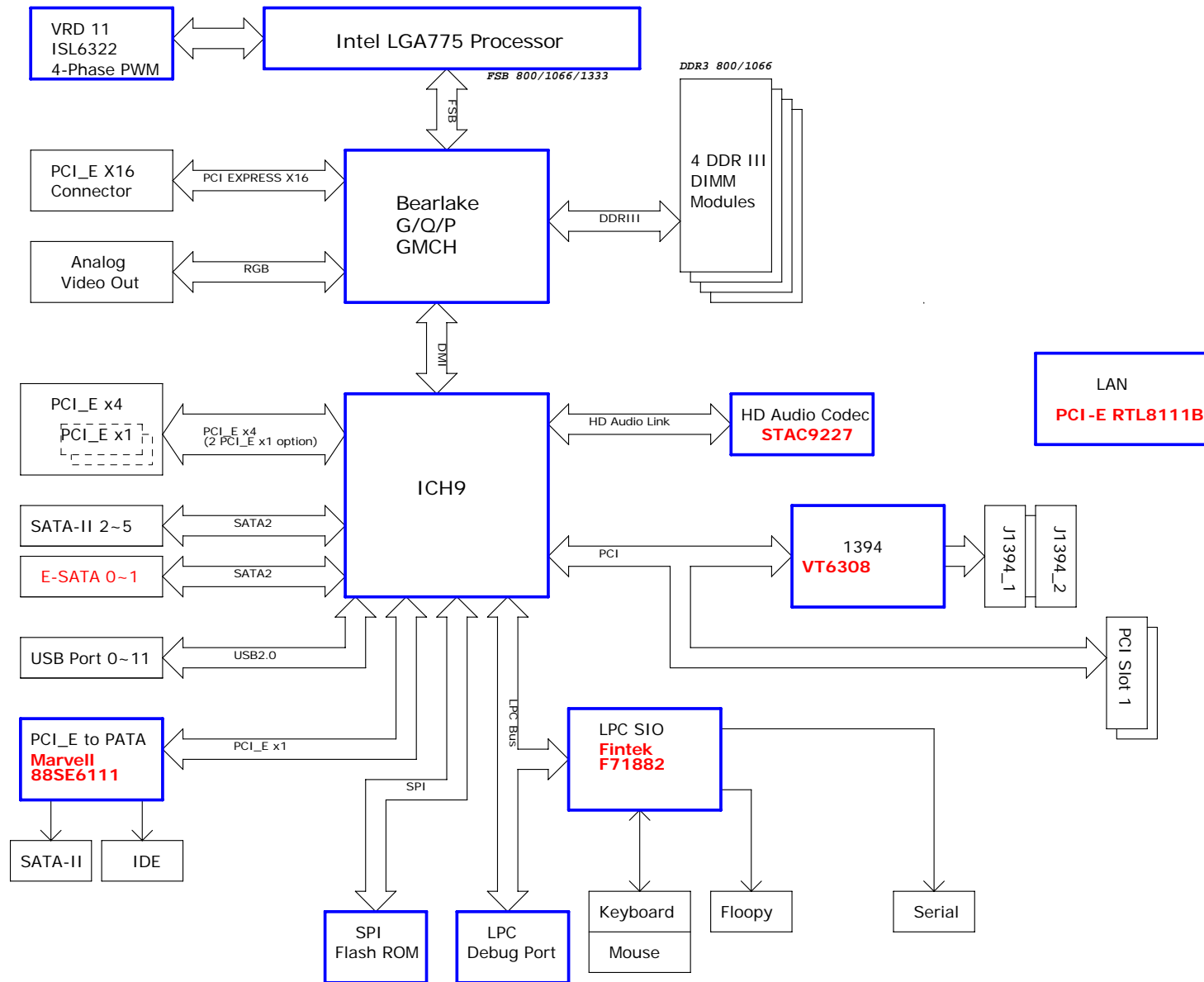
1	Cover Sheet
2	Block Diagram
3	Clock Generate - ICS9LPRS906
4	Intel LGA775 - Signals
5	Intel LGA775 - Power
6	Intel LGA775 - GND
7	Intel Bearlake - FSB / PCIE / VGA / DMI
8	Intel Bearlake - Memory
9	Intel Bearlake - Power
10	Intel Bearlake - GND
11	DDR III DIMM 1 Channel A
12	DDR III DIMM 2 Channel B
13	ICH9 - PCI / DMI / USB / PCIE
14	ICH9 - CPU / SATA / RTC / MSIC
15	ICH7 - POWER / GND
16	PCI - Express X16 Slot / X4 Slot
17	PCI - Express X1 Slot
18	PCI Slot 1 / PCI Slot 2
19	PCI - Express LAN RTL8111B
20	PCI - Express IDE / SATA - 88SE6111
21	PCI IEEE-1394 VT6308
22	Azalia Code ALC888
23	LPC I/O - F71882FG
24	On Board VGA Connector
25	USB Connector
26	FDD / IDE / SATA / eSATA / FANConnector
27	VRM 11 - ISL6322CR
28	ACPI Controller UPI
29	UPI Switch Power
30	ATX POWER / Panel / SMBUS ISO

2007.02.16

MODEL Config.	ORCAD Config.	Function	Option	ERP Number	PCB	
MS7356 STD	cfg7356-std	Intel G33(A1) + ICH9R(A1) + IEEE1394 + ALC888	STD	601-7356-B10.001	Red v0B	CH
MS7356 A	cfg7356-a	Intel P35(A1) + ICH9R(A1) + IEEE1394 + ALC888T	A	601-7356-B20.001	Red v0B	CH

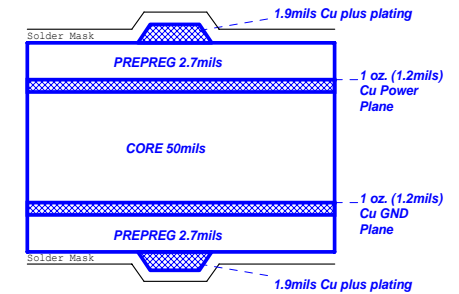
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Title			
Cover Sheet			
Size	Document Number	Rev	
Custom	MS-7356	0B	
Date:	Monday, February 26, 2007	Sheet	1 of 36

Block Diagram

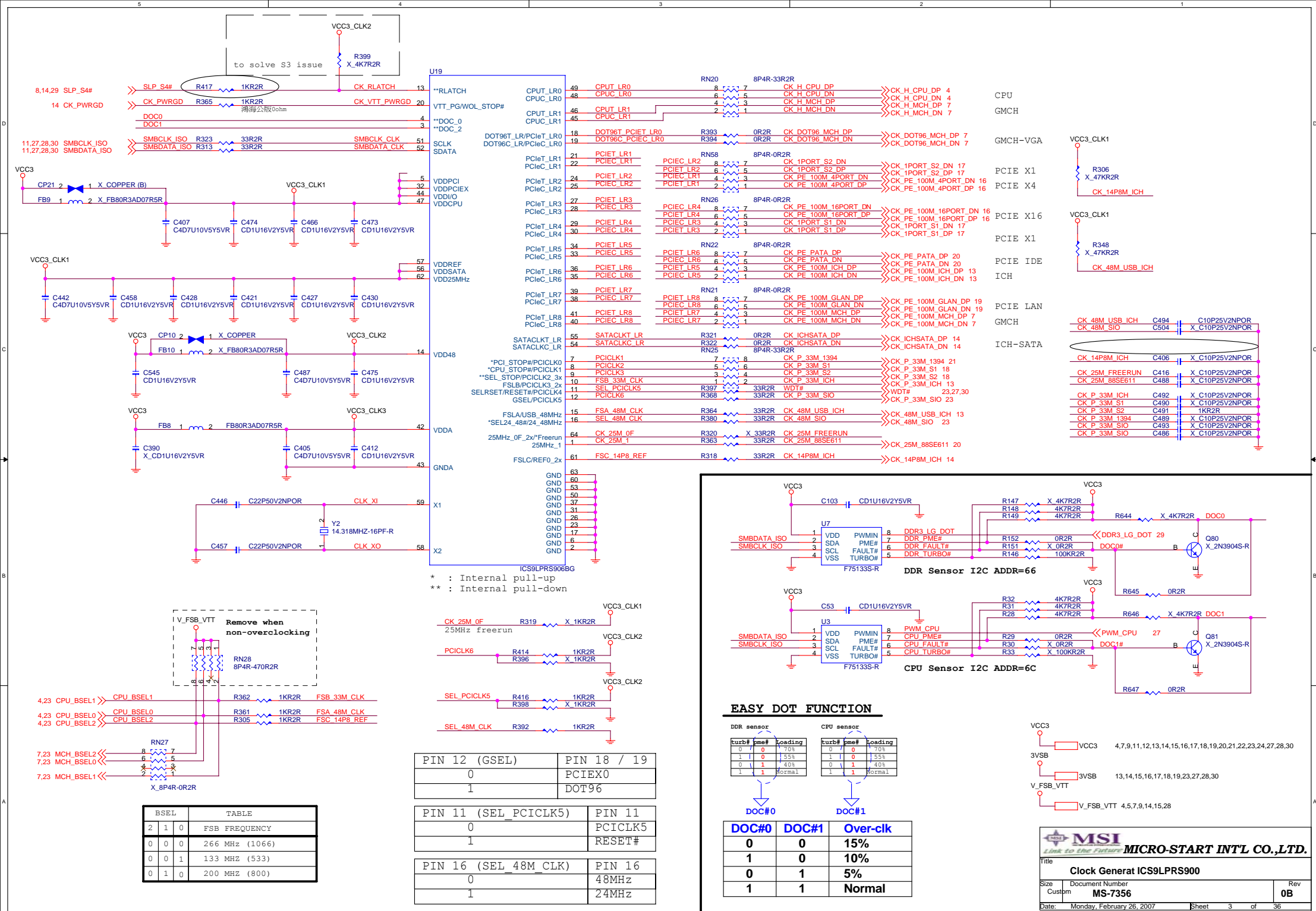


Board Stack-up

(1080 Prepreg Considerations)



Single End 50ohm Top/Bottom : 4mils
 USB2.0 - 90ohm : 15/4.5/7.5/4.5/15
 SATA - 95ohm : 15/4/8/4/15
 LAN - 100ohm : 15/4/8/4/15
 PCIE - 95ohm : 15/4/8/4/15
 IEEE1394 - 110ohm : 15/4/9/4/15
 IDE : 15/4/8/4/15



CPU SIGNAL BLOCK

7 H_A# [3..35] << H_A# [3..35]
 MCERR# Chipset does not support this signal
 BINIT# Chipset does not support this signal

7 H_DB# [0..3] << H_DB# [0..3]

5 H_IERR# << H_IERR#
 14 H_FERR# << H_FERR#
 14 H_STPOLK# << H_STPOLK#
 14 H_INIT# << H_INIT#
 7 H_DBSY# << H_DBSY#
 7 H_DRDY# << H_DRDY#
 7 H_TRDY# << H_TRDY#
 7 H_ADS# << H_ADS#
 7 H_LOCK# << H_LOCK#
 7 H_BNR# << H_BNR#
 7 H_HIT# << H_HIT#
 7 H_HITM# << H_HITM#
 7 H_BPR# << H_BPR#
 7 H_DEFER# << H_DEFER#

14,23 PECI << PECI
 23 VTI# << VTI#
 14 GNDHM << GNDHM
 14 H_TRMTRIP# << H_TRMTRIP#
 23 SKTOCC# << SKTOCC#
 5 H_PROCHOT# << H_PROCHOT#
 14 H_IGNNE# << H_IGNNE#
 14 ICH_H_SMI# << ICH_H_SMI#
 14 H_A20M# << H_A20M#

VTT_OUT_LEFT
 R129 51R2FR
 C100 CD1U16V2Y5VR
 BOOTSELECT 51ohm

3,23 CPU_BSEL0 << CPU_BSEL0
 3,23 CPU_BSEL1 << CPU_BSEL1
 3,23 CPU_BSEL2 << CPU_BSEL2
 5,14 H_PWRGD << H_PWRGD
 5,7 H_CPURST# << H_CPURST#

H_D#63 B22# D63#
 H_D#62 A22# D62#
 H_D#61 B19# D61#
 H_D#59 B21# D59#
 H_D#58 C21# D58#
 H_D#57 B18# D57#
 H_D#56 B16# D56#
 H_D#55 B18# D55#
 H_D#54 C18# D54#

6 H_BPM#0_G1 << H_BPM#0_G1
 H_BPM#1_C9 << H_BPM#1_C9
 H_TESTHI9 << H_TESTHI9
 H_TESTHI8 << H_TESTHI8
 H_TESTHI2 << H_TESTHI2

for Kentsfield

R137 0R2R H_BPM#0
 R90 0R2R H_BPM#1
 R110 0R2R H_BPM#2
 R136 0R2R H_BPM#3
 R119 0R2R H_TESTHI2_U1 << H_TESTHI2_U1

U8A
 A35# A46#
 A34# A45#
 A33# A44#
 A32# A43#
 A31# A42#
 A30# A41#
 A29# A40#
 A28# A39#
 A27# A38#
 A26# A37#
 A25# A36#
 A24# A35#
 A23# A34#
 A22# A33#
 A21# A32#
 A20# A31#
 A19# A30#
 A18# A29#
 A17# A28#
 A16# A27#
 A15# A26#
 A14# A25#
 A13# A24#
 A12# A23#
 A11# A22#
 A10# A21#
 A9# A20#
 A8# A19#
 A7# A18#
 A6# A17#
 A5# A16#
 A4# A15#
 A3# A14#
 A2# A13#
 A1# A12#
 A0# A11#
 A3# A14#
 A2# A13#
 A1# A12#
 A0# A11#
 A3# A14#
 A2# A13#
 A1# A12#
 A0# A11#

AH2 X N5
 AE6 X C9
 D16 X
 A20 X
 Y1
 V2
 AA2

BESEL0 G29
 BESEL1 J40
 BESEL2 G30

RESET# G23

D63#
 D62#
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DBI0# A8#
 DBI1# G11#
 DBI2# D19#
 DBI3# C20#
 IERR# AB2#
 MCERR# AB3#
 FERR# PBE# M3#
 STPOLK# M3#
 BINIT# P3#
 INIT# P3#
 RSP# H4#
 DBSY# B2#
 DRDY# C1#
 TRDY# C2#
 ADS# D2#
 LOCK# C3#
 BNR# C2#
 HIT# D4#
 HITM# E4#
 BPR# G8#
 DEFER# G7#
 TDI AD1#
 TDO AF1#
 TMS AC1#
 TRST# AG1#
 TCK AE1#
 AL1#
 AK1#
 M2#
 AE8#
 AL2#
 N2#
 P2#
 K3#
 L2#
 RSVD#AH2 X N5
 RESERVED0 X AE6
 RESERVED1 C9
 RESERVED2 D16
 RESERVED4 A20
 RESERVED5 Y1
 BOOTSELECT V2
 LL_ID1 AA2

BESEL0 G29
 BESEL1 J40
 BESEL2 G30

RESET# G23

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DBR# AC2#
 VCC_SENSE AN3#
 VSS_SENSE AN4#
 VCC_MB_REGULATION AN6#
 VSS_MB_REGULATION AN6#
 ITP_CLK1 AB3#
 ITP_CLK0 AB3#
 RSVD#VID7 AM7#
 RSVD#VID6 AM6#
 RSVD#VID5 AM5#
 RSVD#VID4 AM4#
 RSVD#VID3 AM3#
 RSVD#VID2 AM2#
 RSVD#VID1 AM1#
 RSVD#VID0 AM0#

BESEL0 G29
 BESEL1 J40
 BESEL2 G30

RESET# G23

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VID_SELECT AN7#
 GTLREF0 H1#
 GTLREF1 H2#
 GTLREF2 H29#
 GTLREF3 F2#
 FC5/CPU_GTLREF2 G10#
 RSVD/CPU_GTLREF3

BESEL0 G29
 BESEL1 J40
 BESEL2 G30

RESET# G23

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BPM5# AG3#
 BPM4# AF2#
 BPM3# AG2#
 BPM2# AD2#
 BPM1# AJ1#
 BPM0# AJ2#
 REQ4# J6#
 REQ3# K6#
 REQ2# M6#
 REQ1# J5#
 REQ0# K4#
 TESTHI12 W2#
 TESTHI11 P1#
 TESTHI10 H5#
 TESTHI9 G4#
 TESTHI8 G3#
 TESTHI7 F24#
 TESTHI6 G24#
 TESTHI5 G25#
 TESTHI4 G26#
 TESTHI3 F25#
 TESTHI2 W3#
 TESTHI1 F26#
 TESTHI0 AK6#
 FORCEPH G6#
 RSVD#G6 G28#
 BCLK1# F28#
 BCLK0# F28#
 RS2# F5#
 RS1# B3#
 RS0# F5#
 TEST-U3 U3#
 TEST-U2 U2#
 BR#0 F3#
 AP#0 U2#
 BR#0 F3#
 COMP5 J2#
 COMP4 R1#
 COMP3 G2#
 COMP2 T1#
 COMP1 A13#
 COMP0 A13#
 DP3# J17#
 DP2# H16#
 DP1# H15#
 DP0# J16#
 ADSTB1# AD5#
 ADSTB0# R6#
 DSTBP3# C12#
 DSTBP2# C19#
 DSTBP1# E12#
 DSTBP0# B9#
 DSTBN3# A16#
 DSTBN2# G20#
 DSTBN1# G12#
 DSTBN0# C8#
 LINT1/NMI L1#
 LINT0/INTR K1#

BESEL0 G29
 BESEL1 J40
 BESEL2 G30

RESET# G23

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VCC_SENSE AN3#
 VSS_SENSE AN4#
 VCC_MB_REGULATION AN6#
 VSS_MB_REGULATION AN6#
 ITP_CLK1 AB3#
 ITP_CLK0 AB3#
 RSVD#VID7 AM7#
 RSVD#VID6 AM6#
 RSVD#VID5 AM5#
 RSVD#VID4 AM4#
 RSVD#VID3 AM3#
 RSVD#VID2 AM2#
 RSVD#VID1 AM1#
 RSVD#VID0 AM0#

BESEL0 G29
 BESEL1 J40
 BESEL2 G30

RESET# G23

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VCC_SENSE AN3#
 VSS_SENSE AN4#
 VCC_MB_REGULATION AN6#
 VSS_MB_REGULATION AN6#
 ITP_CLK1 AB3#
 ITP_CLK0 AB3#
 RSVD#VID7 AM7#
 RSVD#VID6 AM6#
 RSVD#VID5 AM5#
 RSVD#VID4 AM4#
 RSVD#VID3 AM3#
 RSVD#VID2 AM2#
 RSVD#VID1 AM1#
 RSVD#VID0 AM0#

BESEL0 G29
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RESET# G23

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VCC_SENSE AN3#
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 VCC_MB_REGULATION AN6#
 VSS_MB_REGULATION AN6#
 ITP_CLK1 AB3#
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 RSVD#VID7 AM7#
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 RSVD#VID2 AM2#
 RSVD#VID1 AM1#
 RSVD#VID0 AM0#

BESEL0 G29
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RESET# G23

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VCC_SENSE AN3#
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 RSVD#VID1 AM1#
 RSVD#VID0 AM0#

BESEL0 G29
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RESET# G23

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VCC_SENSE AN3#
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BESEL0 G29
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RESET# G23

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VCC_SENSE AN3#
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BESEL0 G29
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RESET# G23

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RESET# G23

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BESEL0 G29
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RESET# G23

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BESEL0 G29
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RESET# G23

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VCC_SENSE AN3#
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 VCC_MB_REGULATION AN6#
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 RSVD#VID0 AM0#

BESEL0 G29
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RESET# G23

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VCC_SENSE AN3#
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 VCC_MB_REGULATION AN6#
 VSS_MB_REGULATION AN6#
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 ITP_CLK0 AB3#
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 RSVD#VID6 AM6#
 RSVD#VID5 AM5#
 RSVD#VID4 AM4#
 RSVD#VID3 AM3#
 RSVD#VID2 AM2#
 RSVD#VID1 AM1#
 RSVD#VID0 AM0#

BESEL0 G29
 BESEL1 J40
 BESEL2 G30

RESET# G23

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VCC_SENSE AN3#
 VSS_SENSE AN4#
 VCC_MB_REGULATION AN6#
 VSS_MB_REGULATION AN6#
 ITP_CLK1 AB3#
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 RSVD#VID7 AM7#
 RSVD#VID6 AM6#
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 RSVD#VID4 AM4#
 RSVD#VID3 AM3#
 RSVD#VID2 AM2#
 RSVD#VID1 AM1#
 RSVD#VID0 AM0#

BESEL0 G29
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 BESEL2 G30

RESET# G23

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VCC_SENSE AN3#
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 VCC_MB_REGULATION AN6#
 VSS_MB_REGULATION AN6#
 ITP_CLK1 AB3#
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 RSVD#VID7 AM7#
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 RSVD#VID4 AM4#
 RSVD#VID3 AM3#
 RSVD#VID2 AM2#
 RSVD#VID1 AM1#
 RSVD#VID0 AM0#

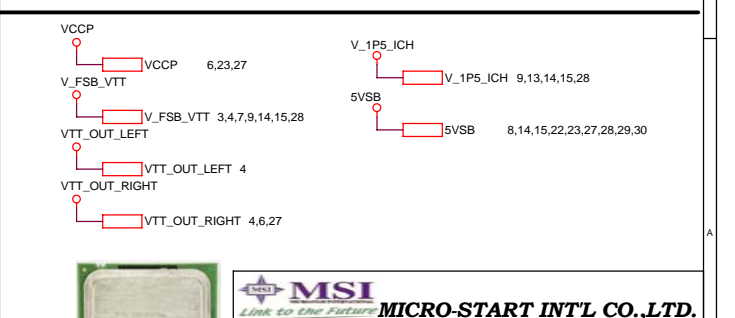
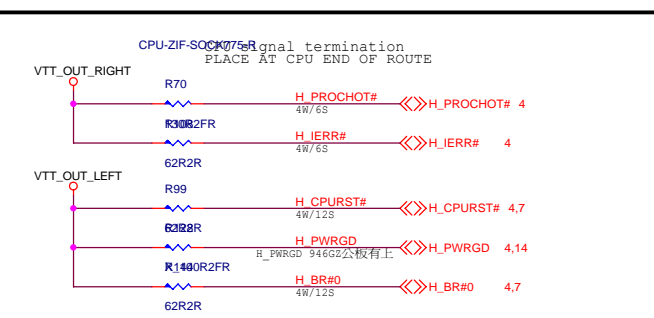
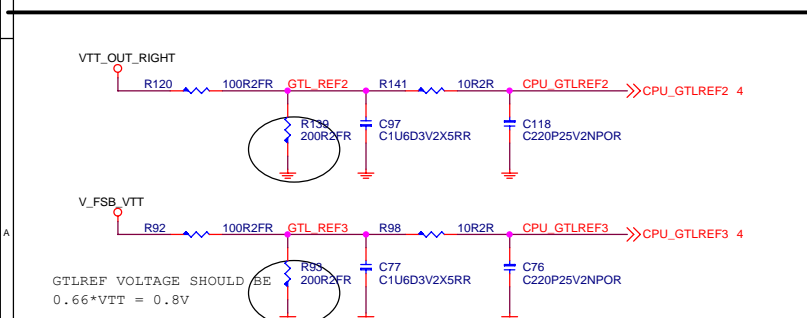
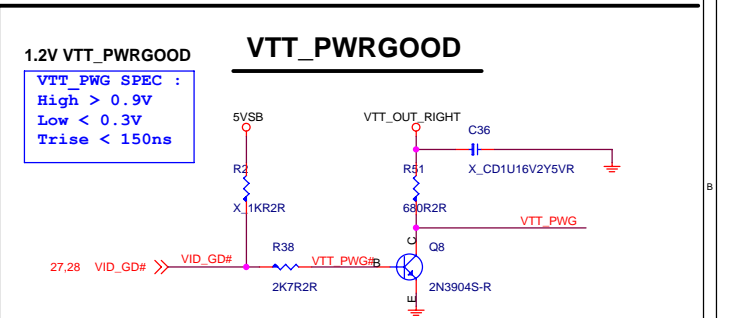
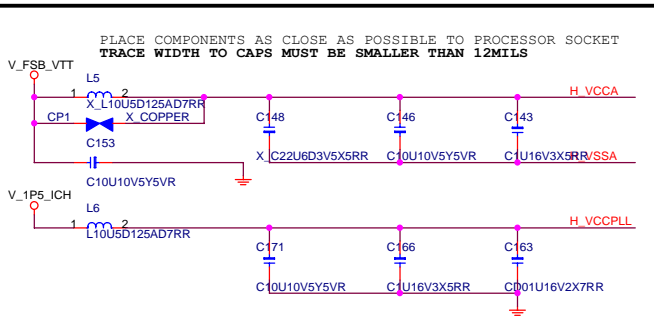
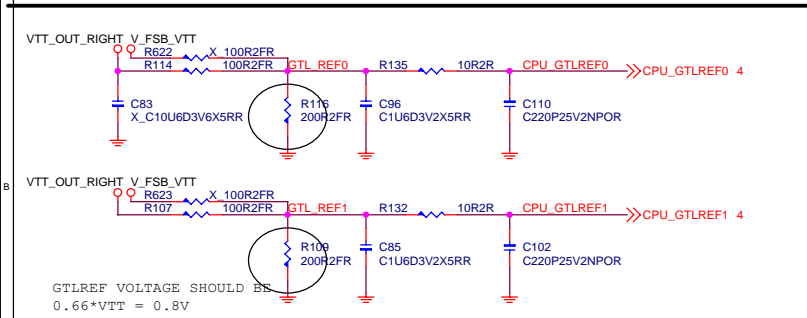
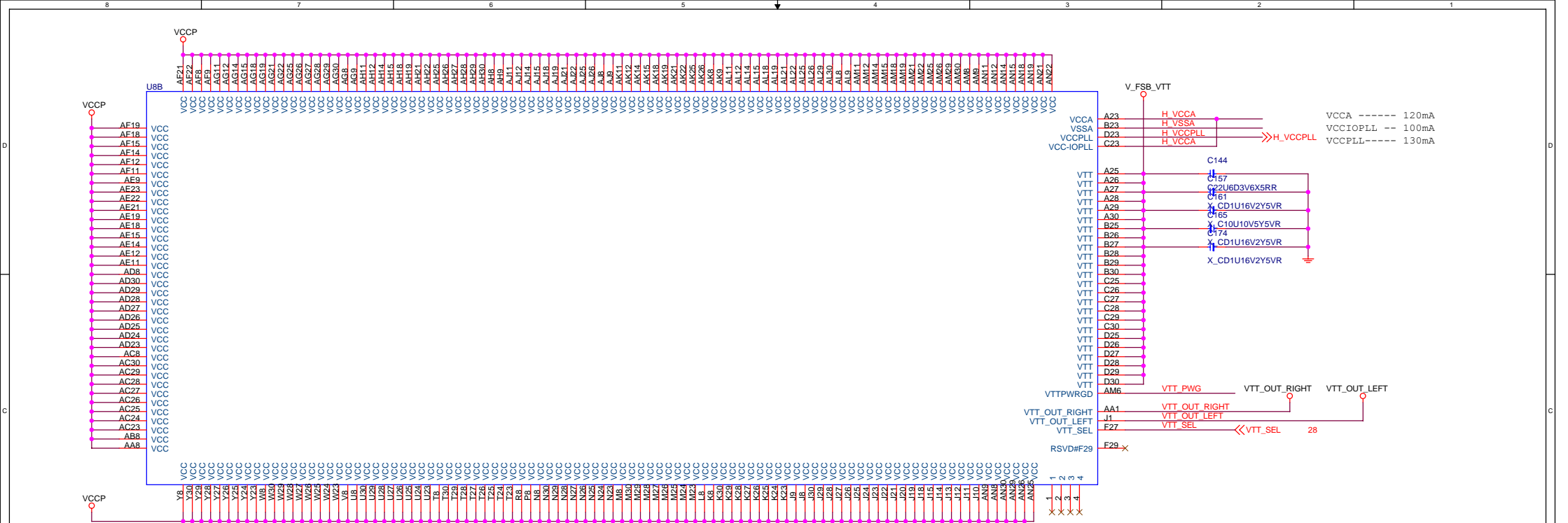
BESEL0 G29
 BESEL1 J40
 BESEL2 G30

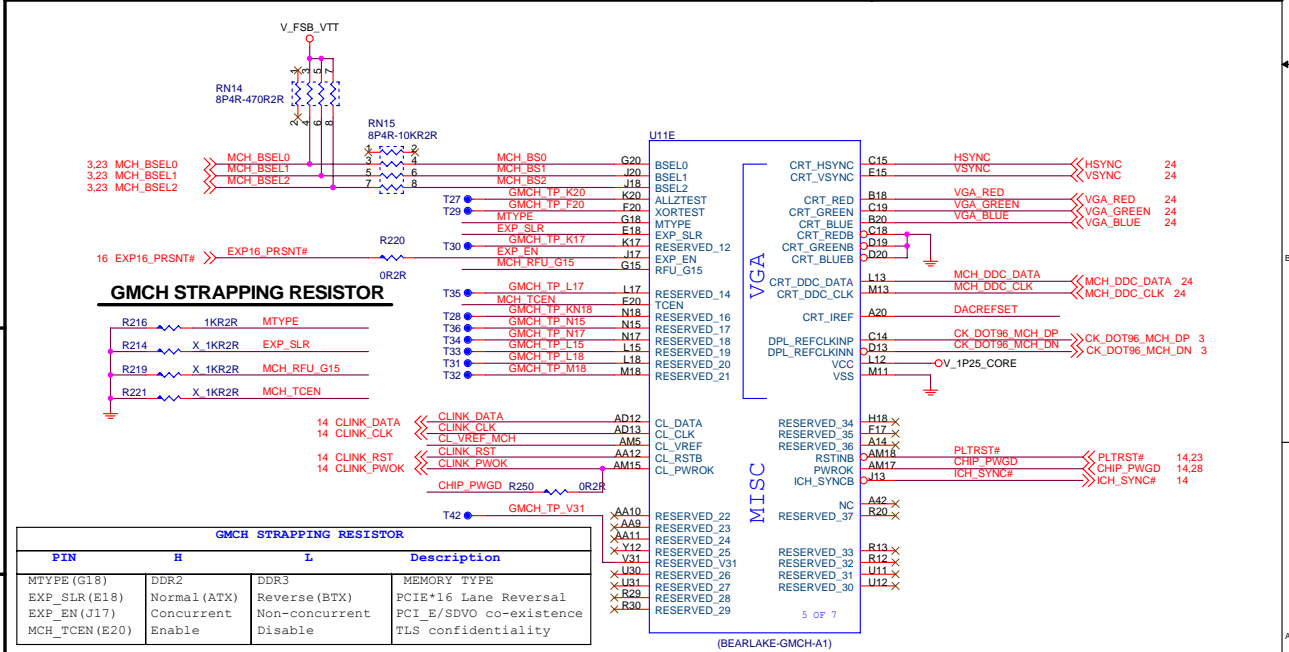
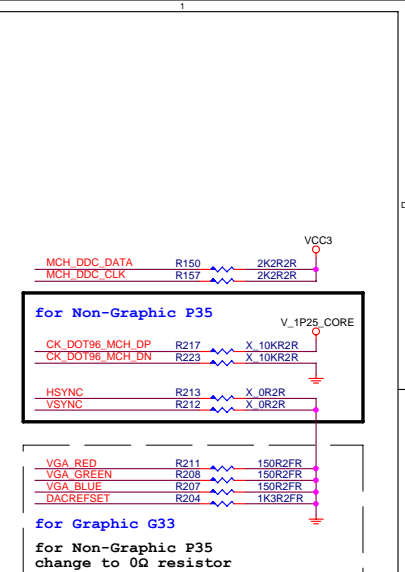
RESET# G23

D63#
 D62#
 D61#
 D59#
 D58#
 D57#
 D56#
 D55#
 D54#

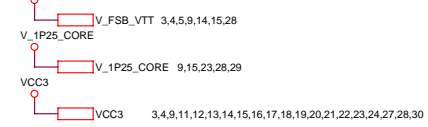
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 D54#

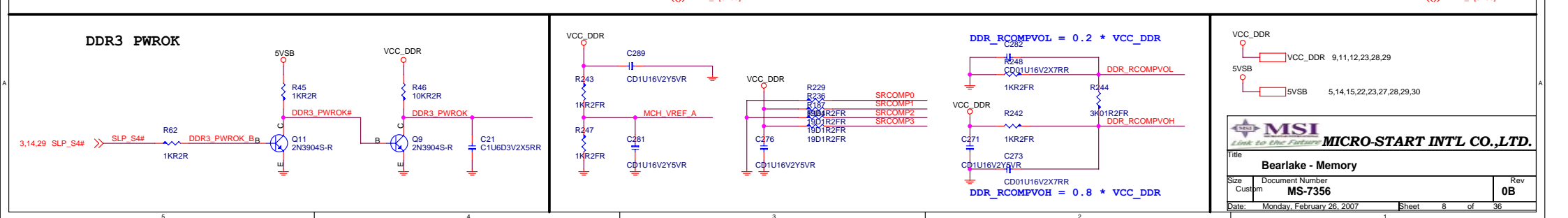
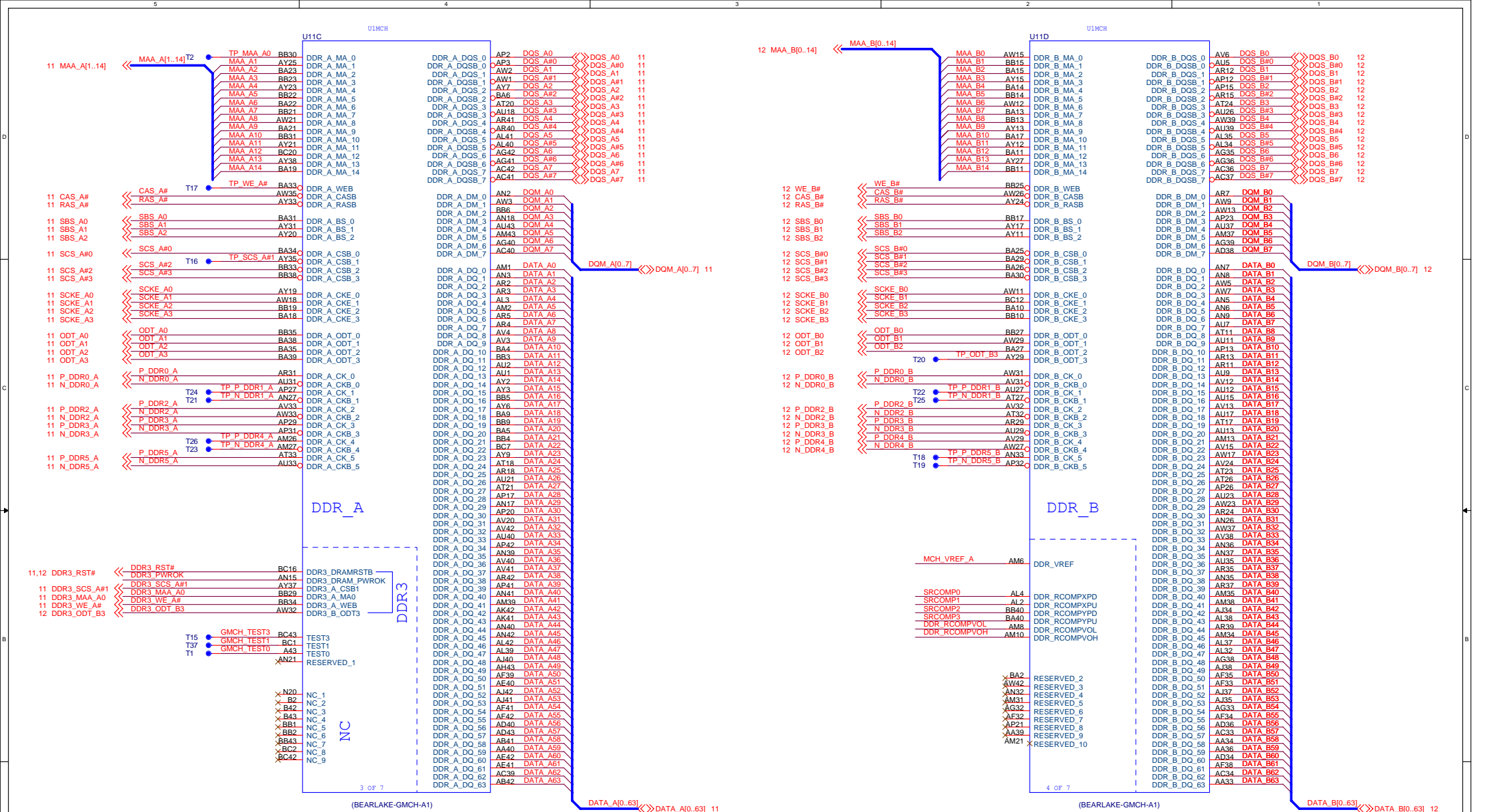
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 VSS_SENSE AN4#
 VCC_MB_REGULATION AN6#
 VSS_MB_REGULATION AN6#
 ITP_CLK1 AB3#
 ITP_CLK0 AB3#
 RSVD#VID7 AM7#
 RSVD#VID6 AM6#
 RSVD#VID5 AM5#
 RSVD#VID4 AM4#
 RSVD#VID3 AM3#
 RSVD#VID2 AM2#
 RSVD#VID1 AM1#
 RSVD#VID0 AM0#

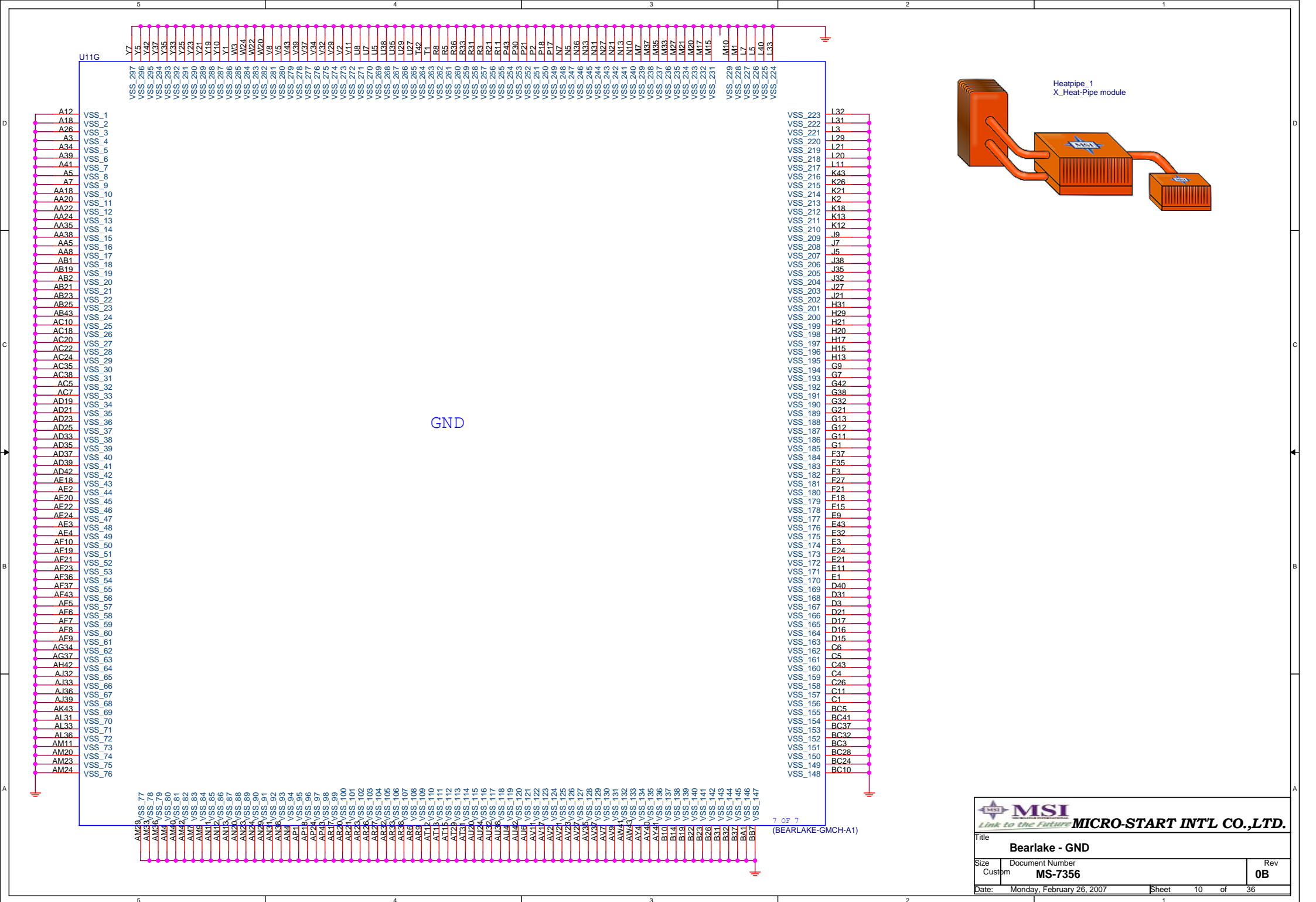




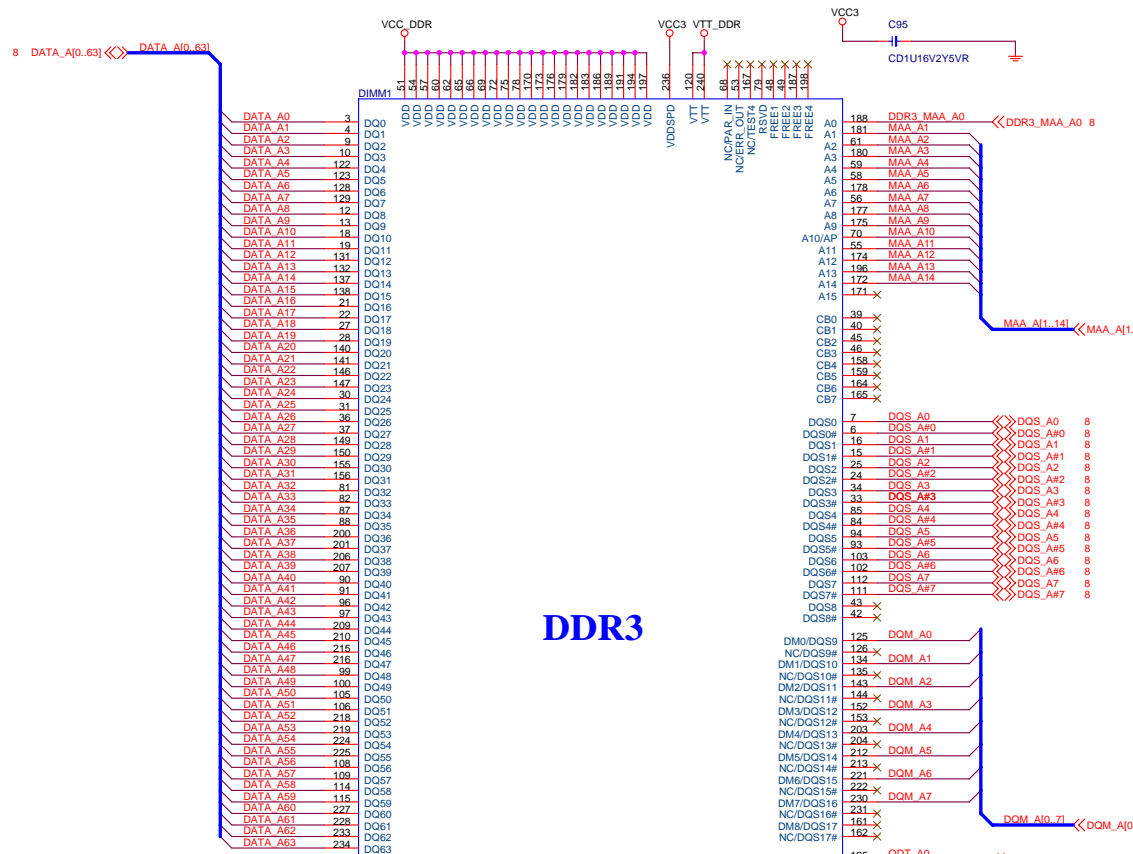
GMCH STRAPPING RESISTOR			
PIN	H	L	Description
MTYPE (G18)	DDR2	DDR3	MEMORY TYPE
EXP_SLR(E18)	Normal (ATX)	Reverse (BTX)	PCIe*16 Lane Reversal
EXP_EN(J17)	Concurrent	Non-concurrent	ECI_S/EDVO co-existence
MCH_TCEN(E20)	Enable	Disable	TLS confidentiality



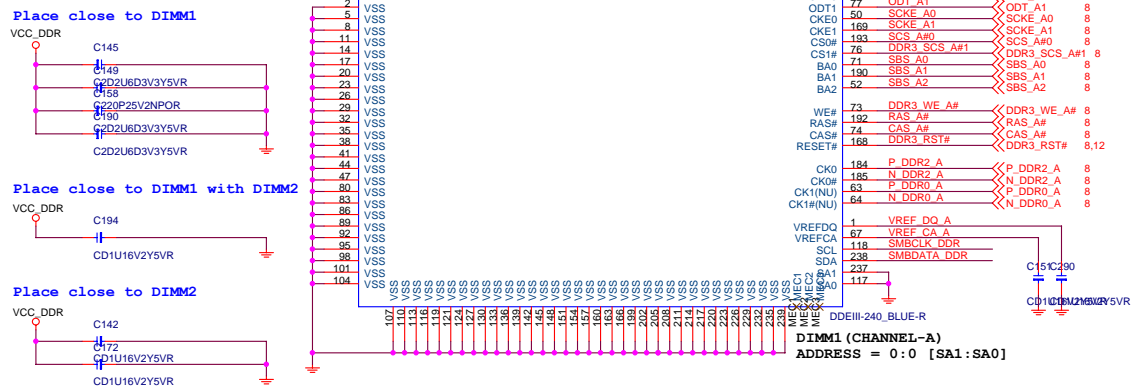




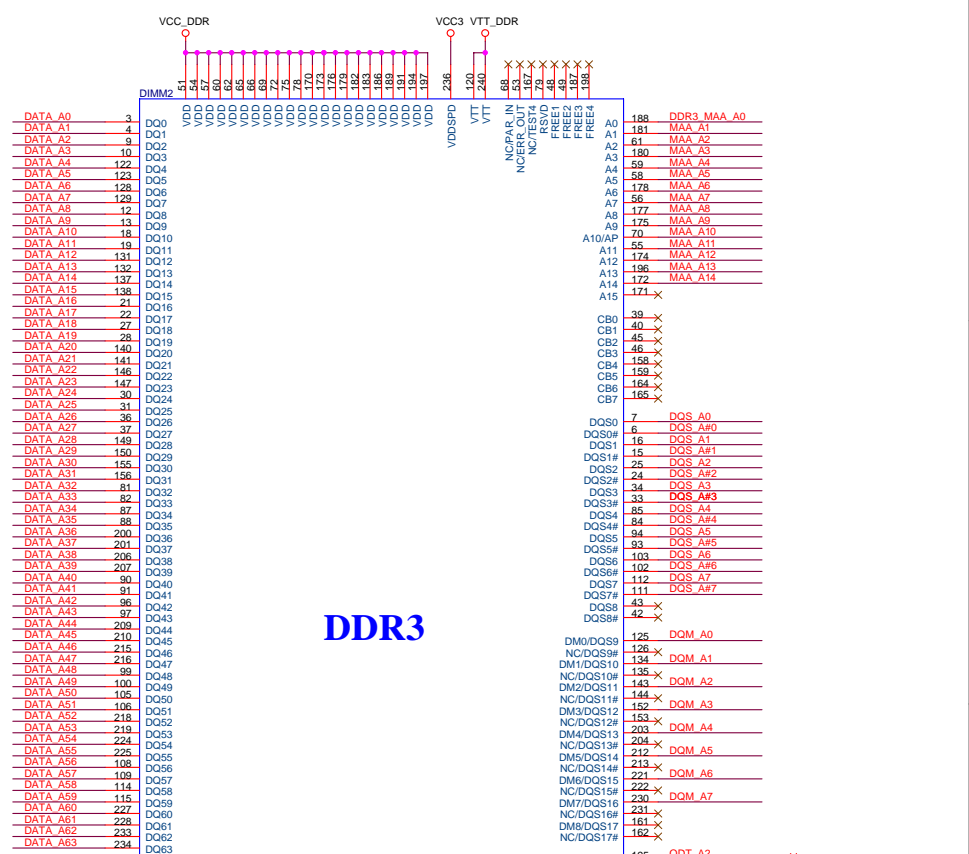
DDRIII DIMM_A1



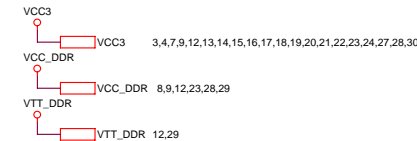
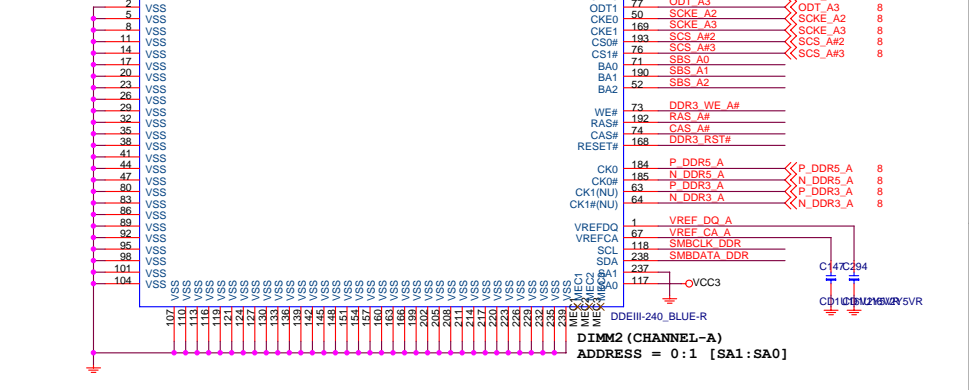
DDR3



DDRIII DIMM_A2



DDR3



DDR3 DIMM B1

DIMM3 (CHANNEL-B)
ADDRESS = 1:0 [SA1:SA0]

Pinout Details:

- DATA_B0[0..63]:** 64-bit data bus, pins 1-63 (odd numbers).
- DATA_B1[0..63]:** 64-bit data bus, pins 64-127 (even numbers).
- DATA_B2[0..63]:** 64-bit data bus, pins 128-191 (odd numbers).
- DATA_B3[0..63]:** 64-bit data bus, pins 192-255 (even numbers).
- VCC_DDR:** Power supply, pins 2, 5, 11, 14, 17, 20, 23, 26, 29, 32, 35, 38, 41, 44, 47, 50, 53, 56, 59, 62, 65, 68, 71, 74, 77, 80, 83, 86, 89, 92, 95, 98, 101, 104, 107, 110, 113, 116, 119, 122, 125, 128, 131, 134, 137, 140, 143, 146, 149, 152, 155, 158, 161, 164, 167, 170, 173, 176, 179, 182, 185, 188, 191, 194, 197, 200, 203, 206, 209, 212, 215, 218, 221, 224, 227, 230, 233, 236, 239, 242, 245, 248, 251, 254.
- VTT_VTT_DDR:** Termination voltage, pins 120, 123, 126, 129, 132, 135, 138, 141, 144, 147, 150, 153, 156, 159, 162, 165, 168, 171, 174, 177, 180, 183, 186, 189, 192, 195, 198, 201, 204, 207, 210, 213, 216, 219, 222, 225, 228, 231, 234, 237, 240, 243, 246, 249, 252, 255.
- Control Signals:**
 - CS#:** Chip select, pins 76, 152, 228.
 - RAS#:** Row address strobe, pins 77, 153, 229.
 - WE#:** Write enable, pins 78, 154, 230.
 - CK0#:** Clock, pins 184, 185, 186, 187, 188, 189, 190, 191, 192, 193, 194, 195, 196, 197, 198, 199, 200, 201, 202, 203, 204, 205, 206, 207, 208, 209, 210, 211, 212, 213, 214, 215, 216, 217, 218, 219, 220, 221, 222, 223, 224, 225, 226, 227, 228, 229, 230, 231, 232, 233, 234, 235, 236, 237, 238, 239, 240, 241, 242, 243, 244, 245, 246, 247, 248, 249, 250, 251, 252, 253, 254, 255.
 - CK1#(NU):** Clock, pins 184, 185, 186, 187, 188, 189, 190, 191, 192, 193, 194, 195, 196, 197, 198, 199, 200, 201, 202, 203, 204, 205, 206, 207, 208, 209, 210, 211, 212, 213, 214, 215, 216, 217, 218, 219, 220, 221, 222, 223, 224, 225, 226, 227, 228, 229, 230, 231, 232, 233, 234, 235, 236, 237, 238, 239, 240, 241, 242, 243, 244, 245, 246, 247, 248, 249, 250, 251, 252, 253, 254, 255.
 - CK1#(NU):** Clock, pins 184, 185, 186, 187, 188, 189, 190, 191, 192, 193, 194, 195, 196, 197, 198, 199, 200, 201, 202, 203, 204, 205, 206, 207, 208, 209, 210, 211, 212, 213, 214, 215, 216, 217, 218, 219, 220, 221, 222, 223, 224, 225, 226, 227, 228, 229, 230, 231, 232, 233, 234, 235, 236, 237, 238, 239, 240, 241, 242, 243, 244, 245, 246, 247, 248, 249, 250, 251, 252, 253, 254, 255.
 - RESET#:** Reset, pins 168, 169, 170, 171, 172, 173, 174, 175, 176, 177, 178, 179, 180, 181, 182, 183, 184, 185, 186, 187, 188, 189, 190, 191, 192, 193, 194, 195, 196, 197, 198, 199, 200, 201, 202, 203, 204, 205, 206, 207, 208, 209, 210, 211, 212, 213, 214, 215, 216, 217, 218, 219, 220, 221, 222, 223, 224, 225, 226, 227, 228, 229, 230, 231, 232, 233, 234, 235, 236, 237, 238, 239, 240, 241, 242, 243, 244, 245, 246, 247, 248, 249, 250, 251, 252, 253, 254, 255.
 - VREFDQ B:** Data bus termination, pins 117, 118, 119, 120, 121, 122, 123, 124, 125, 126, 127, 128, 129, 130, 131, 132, 133, 134, 135, 136, 137, 138, 139, 140, 141, 142, 143, 144, 145, 146, 147, 148, 149, 150, 151, 152, 153, 154, 155, 156, 157, 158, 159, 160, 161, 162, 163, 164, 165, 166, 167, 168, 169, 170, 171, 172, 173, 174, 175, 176, 177, 178, 179, 180, 181, 182, 183, 184, 185, 186, 187, 188, 189, 190, 191, 192, 193, 194, 195, 196, 197, 198, 199, 200, 201, 202, 203, 204, 205, 206, 207, 208, 209, 210, 211, 212, 213, 214, 215, 216, 217, 218, 219, 220, 221, 222, 223, 224, 225, 226, 227, 228, 229, 230, 231, 232, 233, 234, 235, 236, 237, 238, 239, 240, 241, 242, 243, 244, 245, 246, 247, 248, 249, 250, 251, 252, 253, 254, 255.
 - SMBCLK_DDR:** Serial memory bus clock, pins 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 42, 43, 44, 45, 46, 47, 48, 49, 50, 51, 52, 53, 54, 55, 56, 57, 58, 59, 60, 61, 62, 63, 64, 65, 66, 67, 68, 69, 70, 71, 72, 73, 74, 75, 76, 77, 78, 79, 80, 81, 82, 83, 84, 85, 86, 87, 88, 89, 90, 91, 92, 93, 94, 95, 96, 97, 98, 99, 100, 101, 102, 103, 104, 105, 106, 107, 108, 109, 110, 111, 112, 113, 114, 115, 116, 117, 118, 119, 120, 121, 122, 123, 124, 125, 126, 127, 128, 129, 130, 131, 132, 133, 134, 135, 136, 137, 138, 139, 140, 141, 142, 143, 144, 145, 146, 147, 148, 149, 150, 151, 152, 153, 154, 155, 156, 157, 158, 159, 160, 161, 162, 163, 164, 165, 166, 167, 168, 169,

DDR3 DIMM_B2

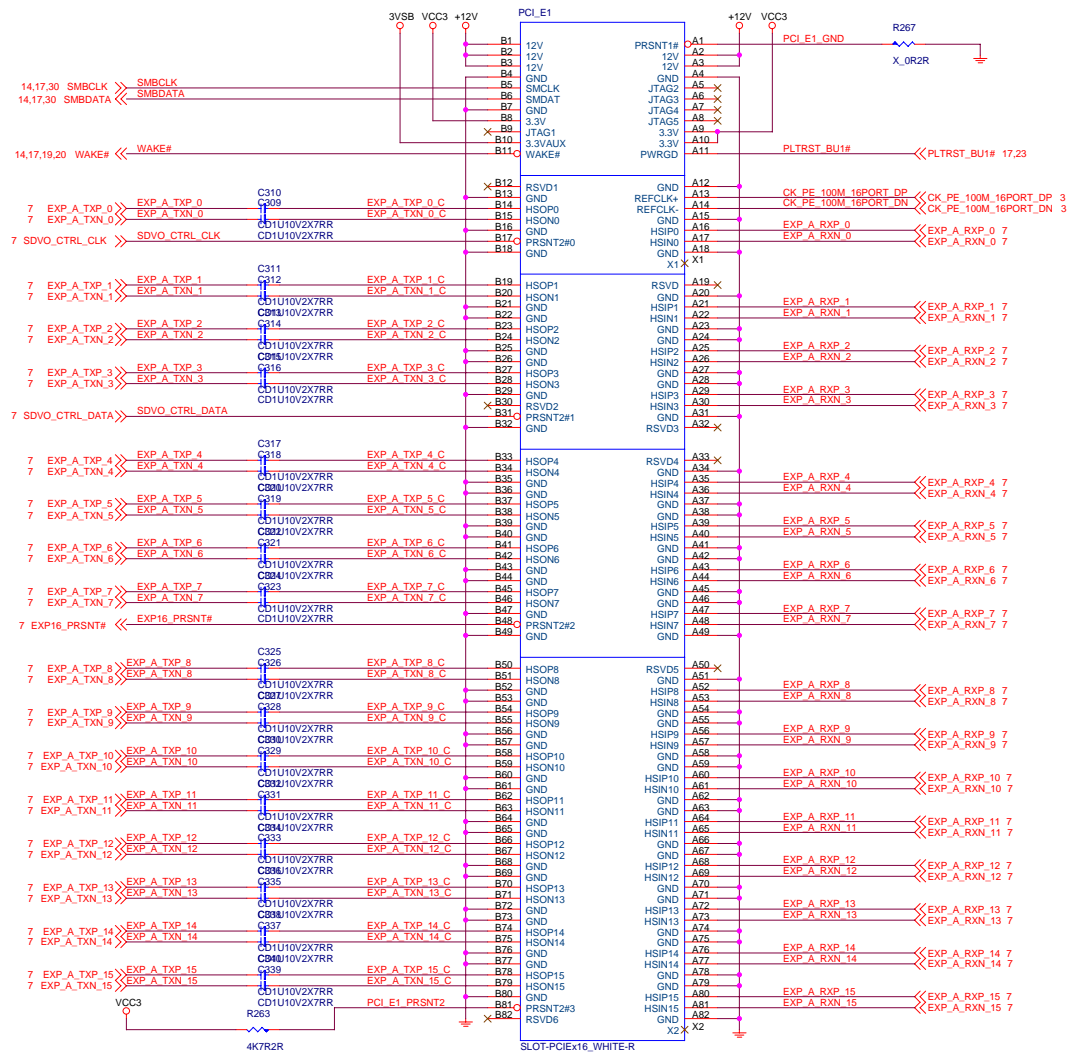
Diagram illustrating the pin connections for a DDR3 DIMM module, showing the DIMM4 (Channel-B) and DIMM3 (Channel-A) configurations. The diagram includes the DIMM pinout, the DIMM4 (Channel-B) pinout, and the DIMM3 (Channel-A) pinout.

DIMM4 (Channel-B) Pinout:

- DATA B0 to DATA B63
- DATA B64 to DATA B127
- DATA B128 to DATA B191
- DATA B192 to DATA B255
- DATA B256 to DATA B319
- DATA B320 to DATA B383
- DATA B384 to DATA B447
- DATA B448 to DATA B511
- DATA B512 to DATA B575
- DATA B576 to DATA B639
- DATA B640 to DATA B703
- DATA B704 to DATA B767
- DATA B768 to DATA B831
- DATA B832 to DATA B895
- DATA B896 to DATA B959
- DATA B960 to DATA B1023
- DATA B1024 to DATA B1087
- DATA B1088 to DATA B1151
- DATA B1152 to DATA B1215
- DATA B1216 to DATA B1279
- DATA B1280 to DATA B1343
- DATA B1344 to DATA B1407
- DATA B1408 to DATA B1471
- DATA B1472 to DATA B1535
- DATA B1536 to DATA B1599
- DATA B1600 to DATA B1663
- DATA B1664 to DATA B1727
- DATA B1728 to DATA B1791
- DATA B1792 to DATA B1855
- DATA B1856 to DATA B1919
- DATA B1920 to DATA B1983
- DATA B1984 to DATA B2047
- DATA B2048 to DATA B2111
- DATA B2112 to DATA B2175
- DATA B2176 to DATA B2239
- DATA B2240 to DATA B2303
- DATA B2304 to DATA B2367
- DATA B2368 to DATA B2431
- DATA B2432 to DATA B2495
- DATA B2496 to DATA B2559
- DATA B2560 to DATA B2623
- DATA B2624 to DATA B2687
- DATA B2688 to DATA B2751
- DATA B2752 to DATA B2815
- DATA B2816 to DATA B2879
- DATA B2880 to DATA B2943
- DATA B2944 to DATA B3007
- DATA B3008 to DATA B3071
- DATA B3072 to DATA B3135
- DATA B3136 to DATA B3199
- DATA B3200 to DATA B3263
- DATA B3264 to DATA B3327
- DATA B3328 to DATA B3391
- DATA B3392 to DATA B3455
- DATA B3456 to DATA B3519
- DATA B3520 to DATA B3583
- DATA B3584 to DATA B3647
- DATA B3648 to DATA B3711
- DATA B3712 to DATA B3775
- DATA B3776 to DATA B3839
- DATA B3840 to DATA B3903
- DATA B3904 to DATA B3967
- DATA B3968 to DATA B4031
- DATA B4032 to DATA B4095
- DATA B4096 to DATA B4159
- DATA B4160 to DATA B4223
- DATA B4224 to DATA B4287
- DATA B4288 to DATA B4351
- DATA B4352 to DATA B4415
- DATA B4416 to DATA B4479
- DATA B4480 to DATA B4543
- DATA B4544 to DATA B4607
- DATA B4608 to DATA B4671
- DATA B4672 to DATA B4735
- DATA B4736 to DATA B4799
- DATA B4800 to DATA B4863
- DATA B4864 to DATA B4927
- DATA B4928 to DATA B4991
- DATA B4992 to DATA B5055
- DATA B5056 to DATA B5119
- DATA B5120 to DATA B5183
- DATA B5184 to DATA B5247
- DATA B5248 to DATA B5311
- DATA B5312 to DATA B5375
- DATA B5376 to DATA B5439
- DATA B5440 to DATA B5503
- DATA B5504 to DATA B5567
- DATA B5568 to DATA B5631
- DATA B5632 to DATA B5695
- DATA B5696 to DATA B5759
- DATA B5760 to DATA B5823
- DATA B5824 to DATA B5887
- DATA B5888 to DATA B5951
- DATA B5952 to DATA B6015
- DATA B6016 to DATA B6079
- DATA B6080 to DATA B6143
- DATA B6144 to DATA B6207
- DATA B6208 to DATA B6271
- DATA B6272 to DATA B6335
- DATA B6336 to DATA B6399
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- DATA B6528 to DATA B6591
- DATA B6592 to DATA B6655
- DATA B6656 to DATA B6719
- DATA B6720 to DATA B6783
- DATA B6784 to DATA B6847
- DATA B6848 to DATA B6911
- DATA B6912 to DATA B6975
- DATA B6976 to DATA B7039
- DATA B7040 to DATA B7103
- DATA B7104 to DATA B7167
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- DATA B8192 to DATA B8255
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- DATA B8896 to DATA B8959
- DATA B8960 to DATA B9023
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- DATA B9088 to DATA B9151
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- DATA B9344 to DATA B9407
- DATA B9408 to DATA B9471
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- DATA B9600 to DATA B9663
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- DATA B9920 to DATA B9983
- DATA B9984 to DATA B10047
- DATA B10048 to DATA B10111
- DATA B10112 to DATA B10175
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- DATA B10880 to DATA B10943
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- DATA B13440 to DATA B13503
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- DATA

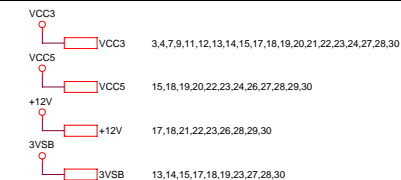
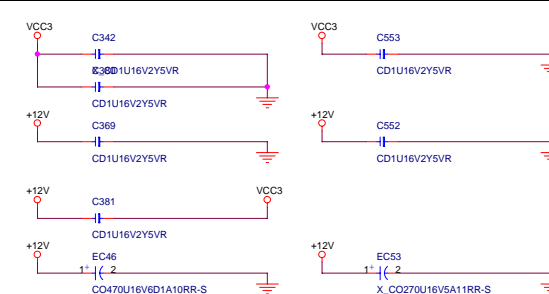
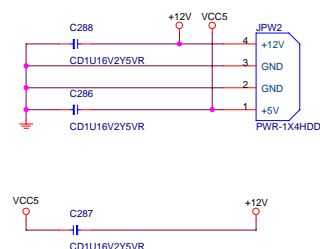
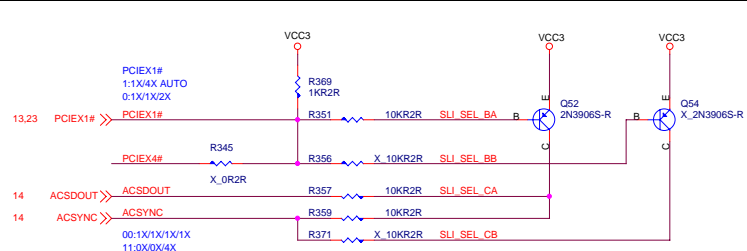
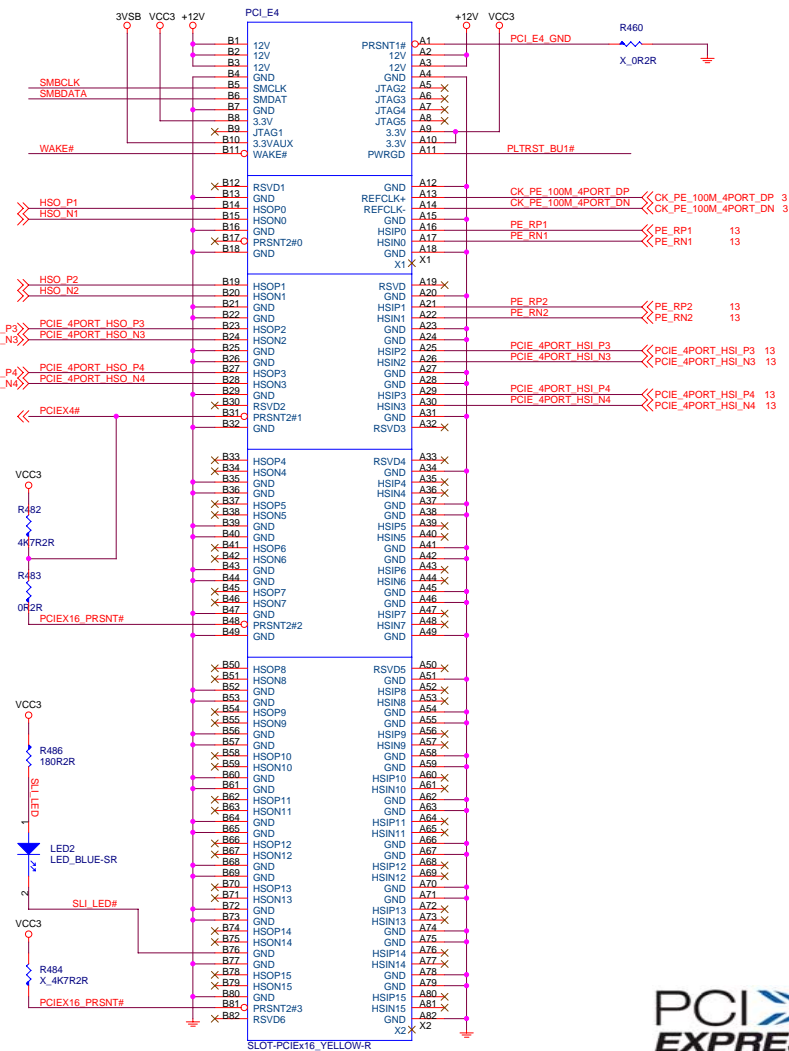
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PCI Express X16 Slot



PCI Express X4 Slot

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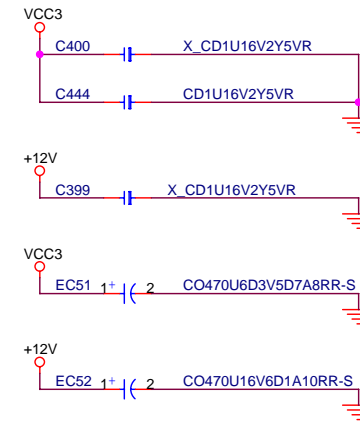
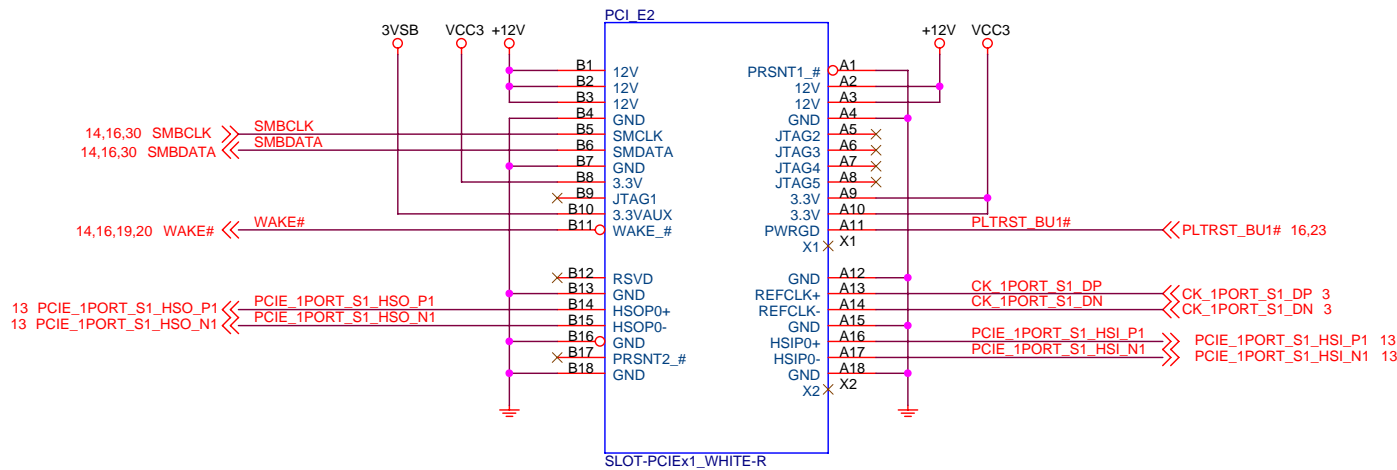
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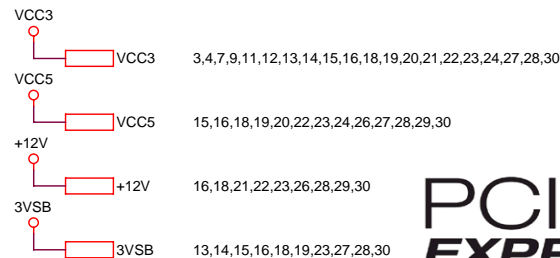
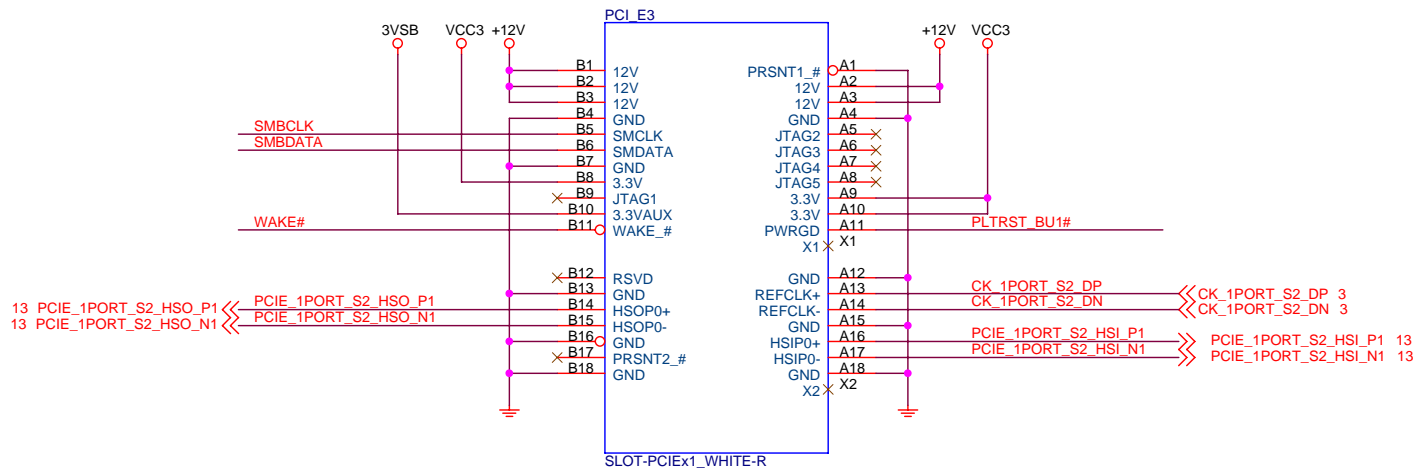
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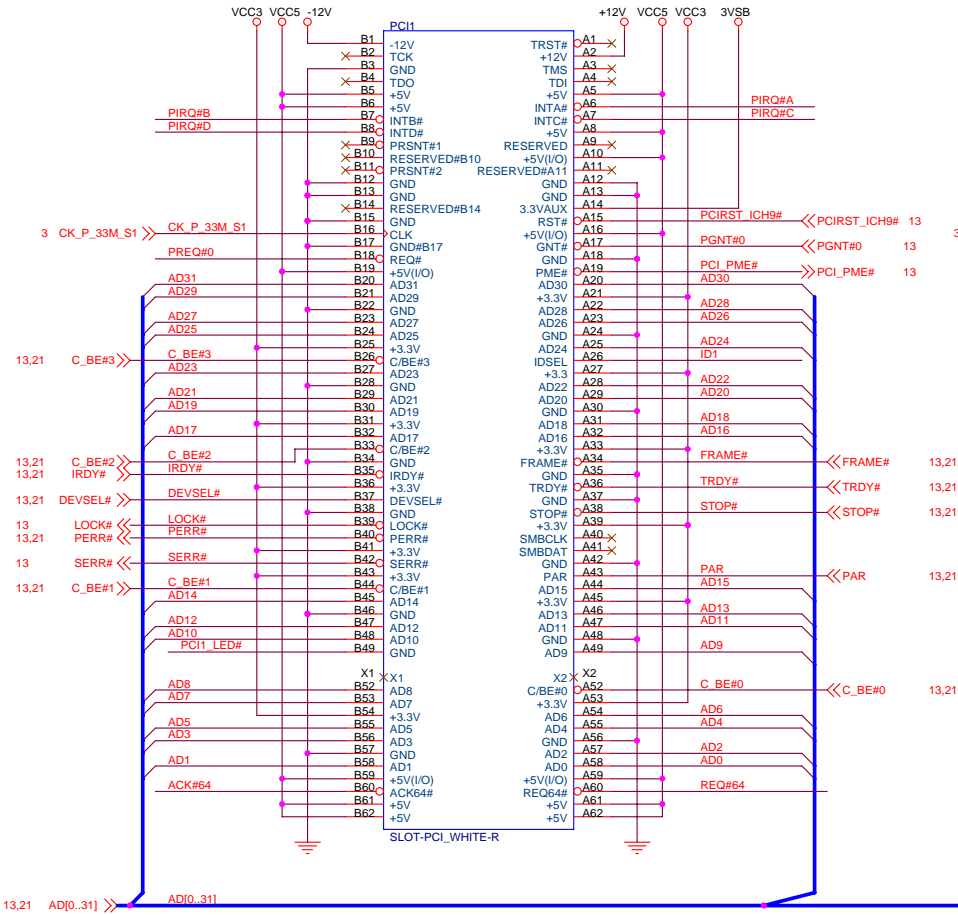


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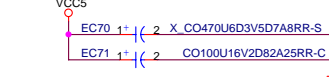
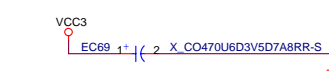
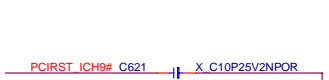
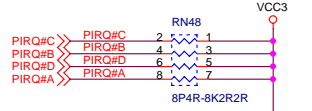
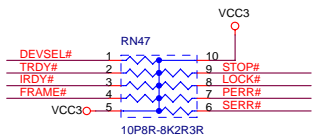
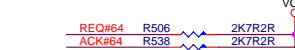
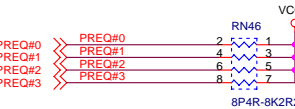
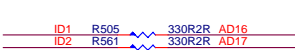
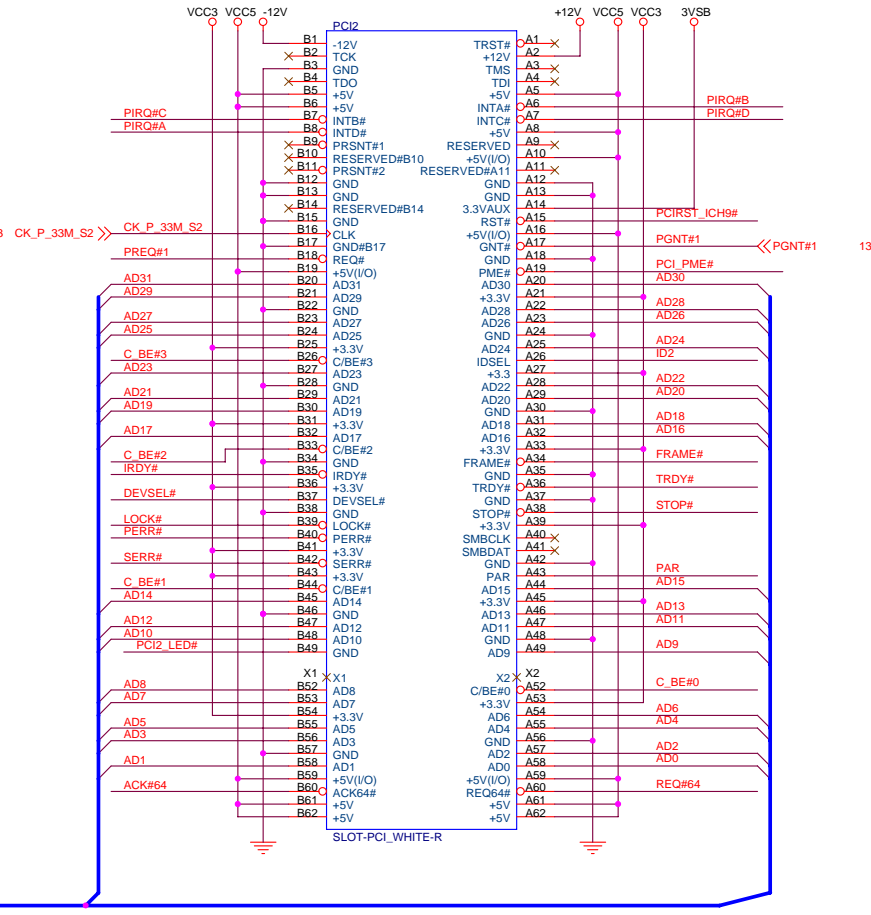


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Date:	Monday, February 26, 2007	Sheet	17 of 36

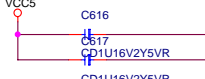
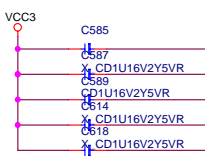
PCI1



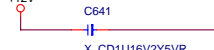
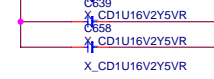
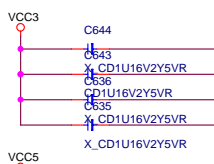
PCI2



Place close to PCI1



Place close to PCI2

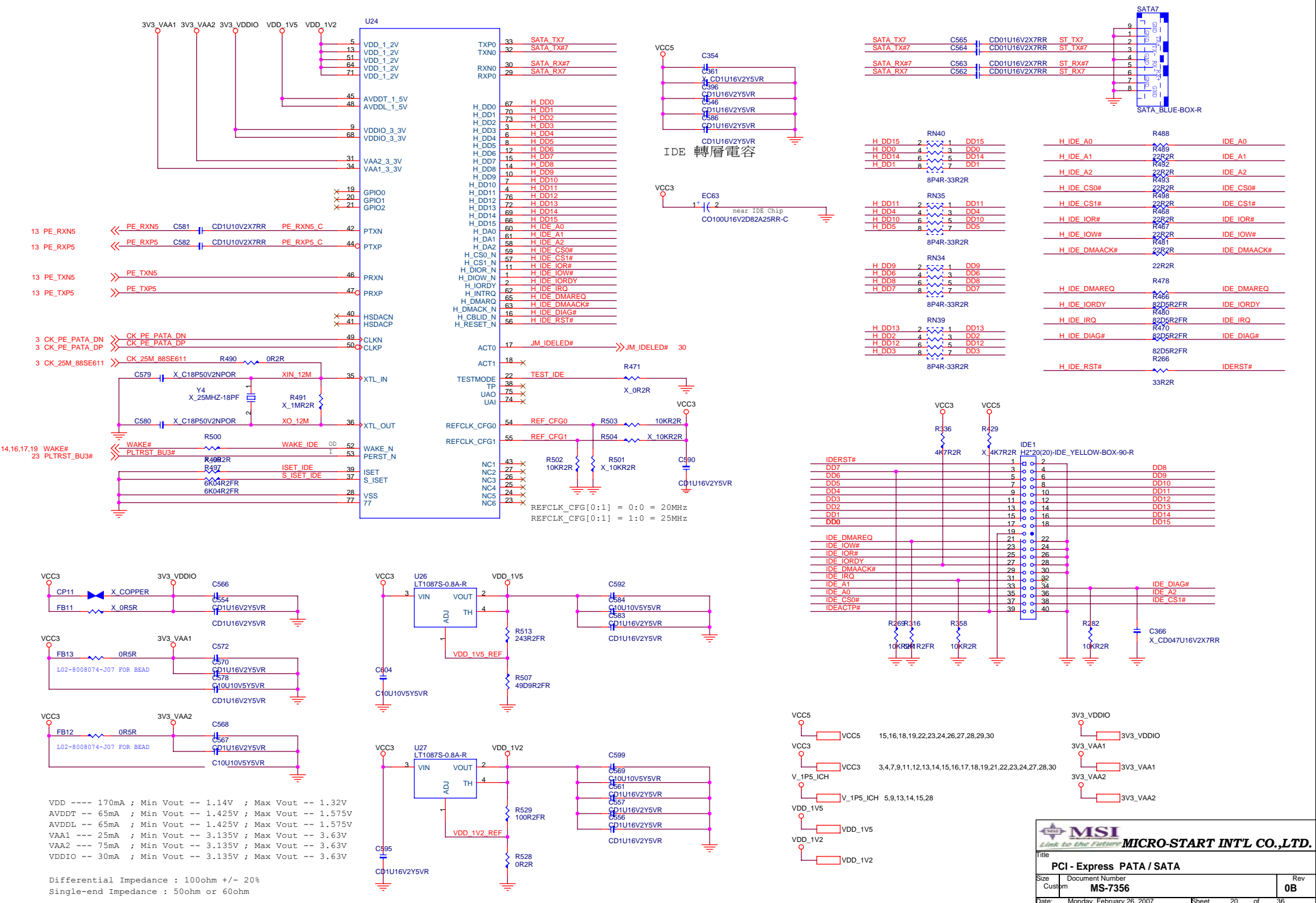


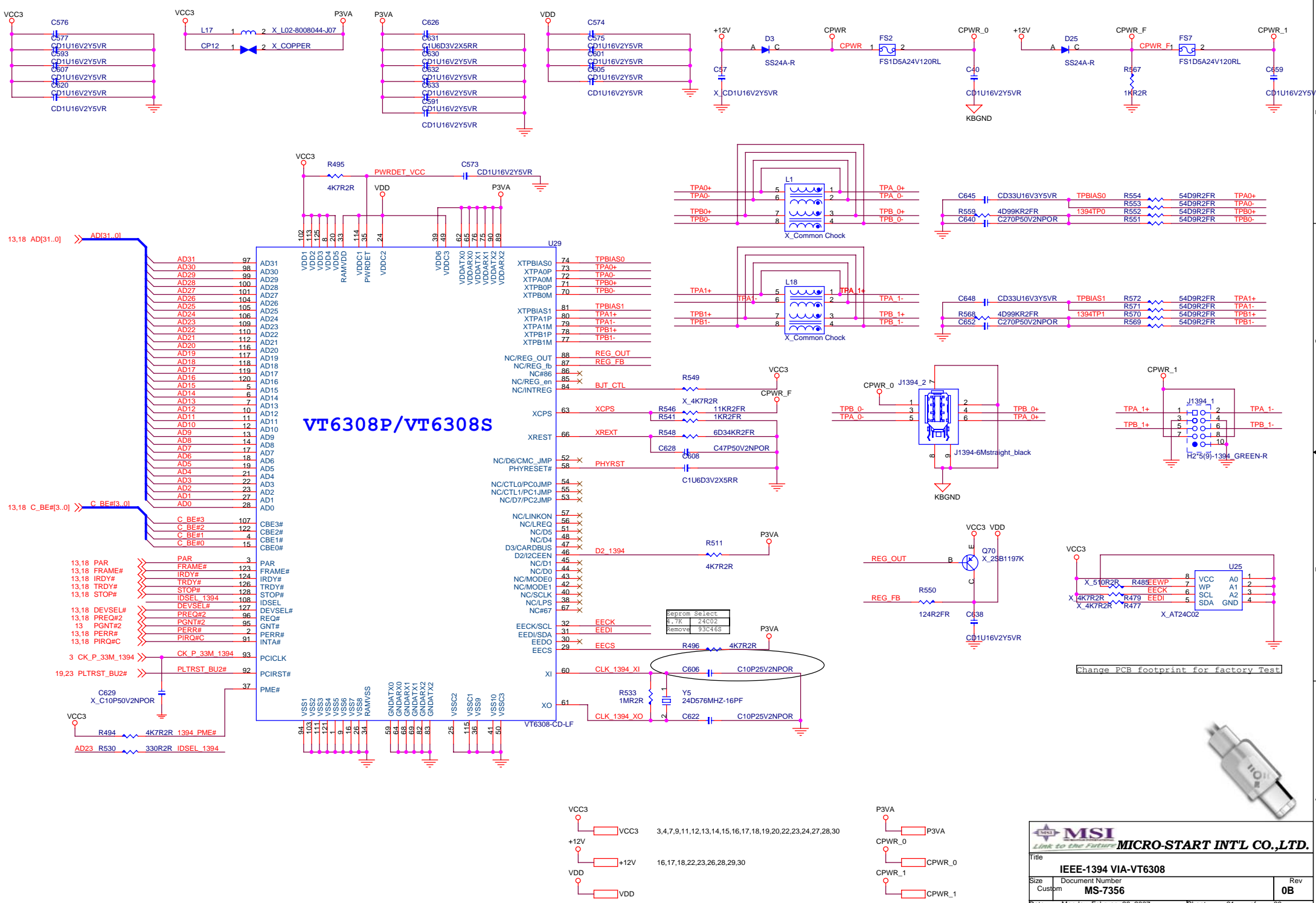
MSI
Link to the Future
MICRO-START INT'L CO.,LTD.

Title: **PCI1 Slot / PCI2 Slot**

Size: Custom
Document Number: **MS-7279**
Rev: **0B**

Date: Monday, February 26, 2007
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VT6308P/VT6308S

Seprom Select	24C02
Remove	93C46S

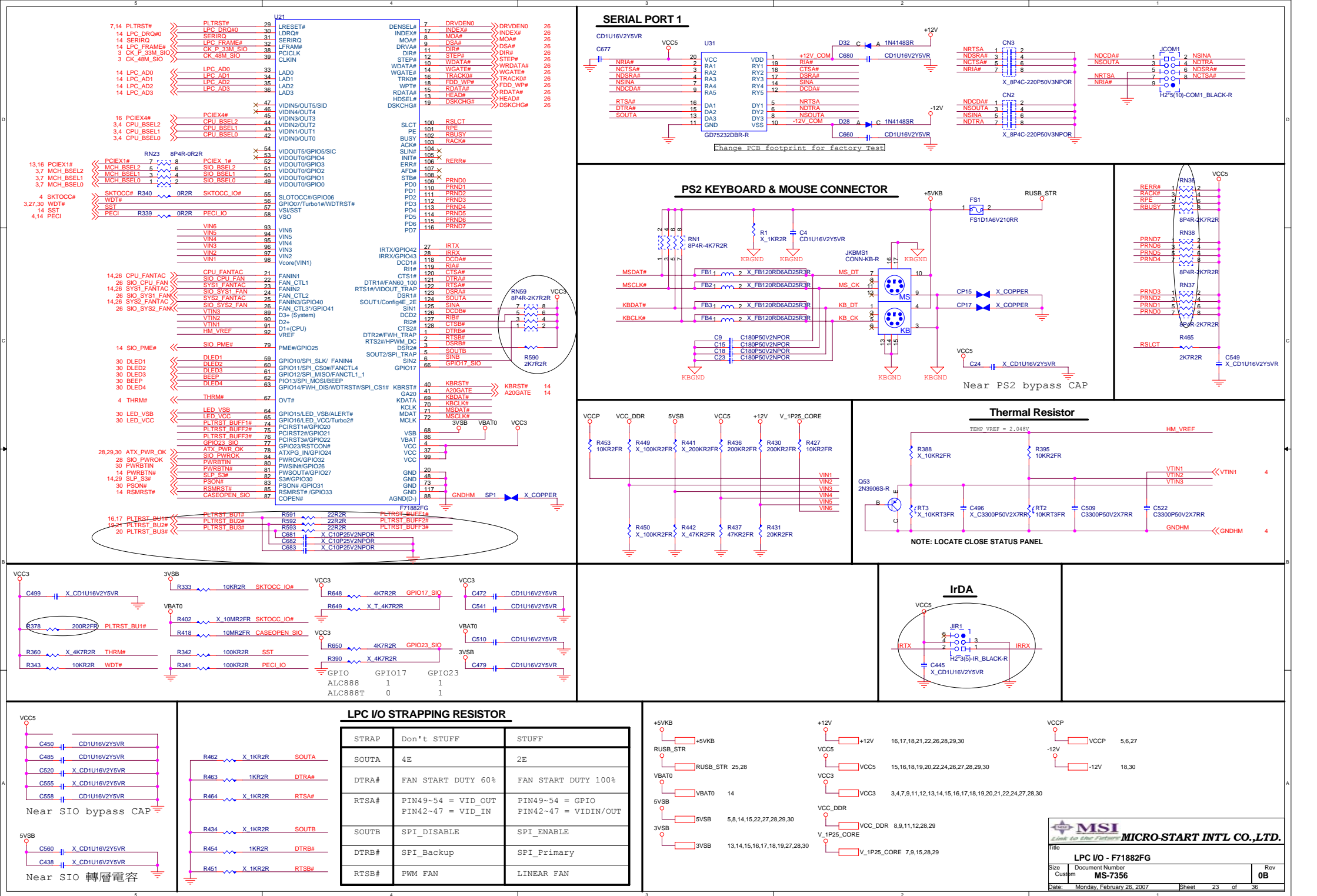
Change PCB footprint for factory Test

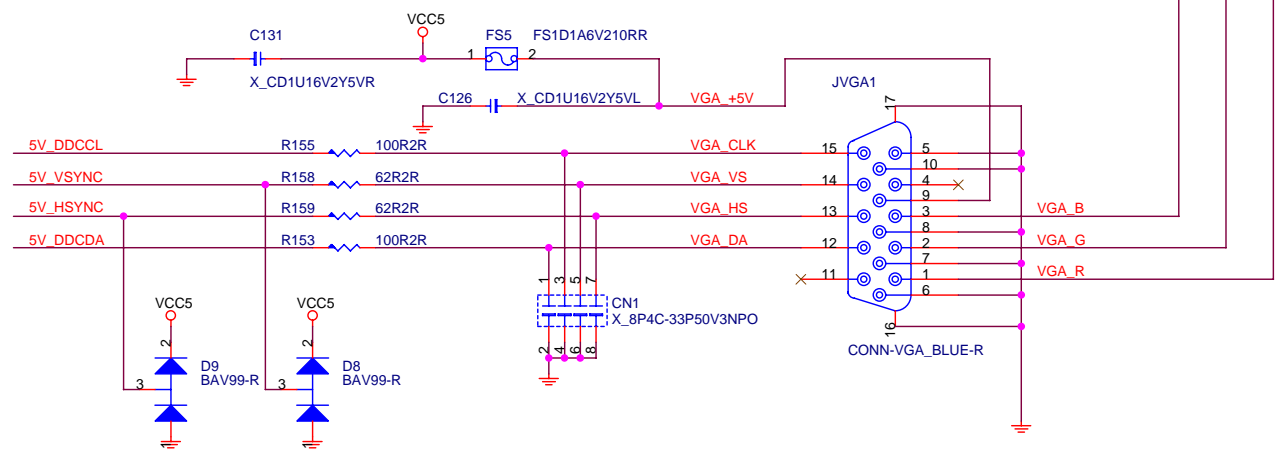
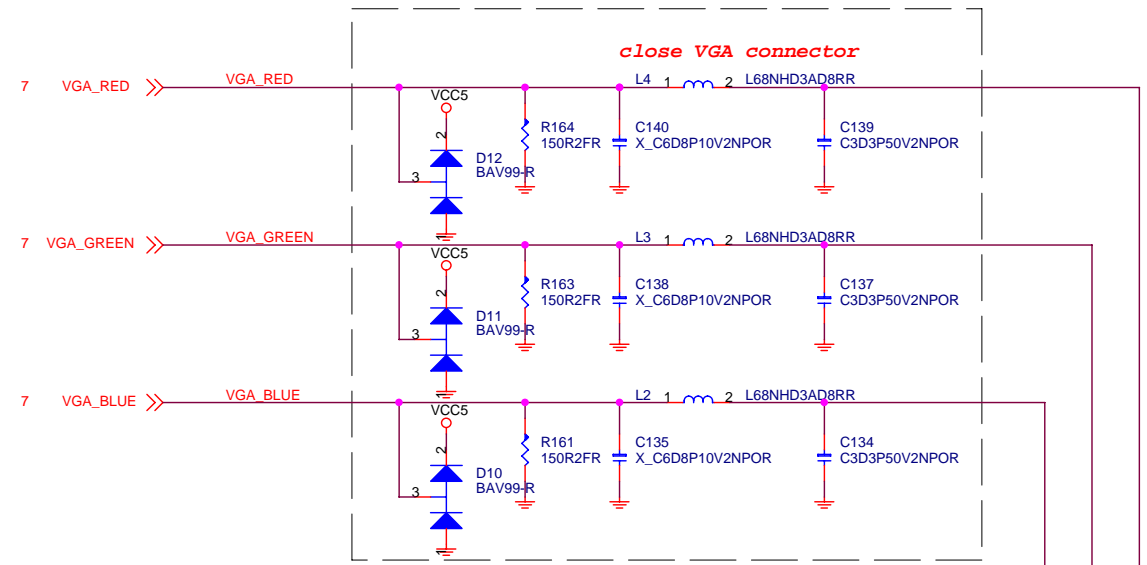
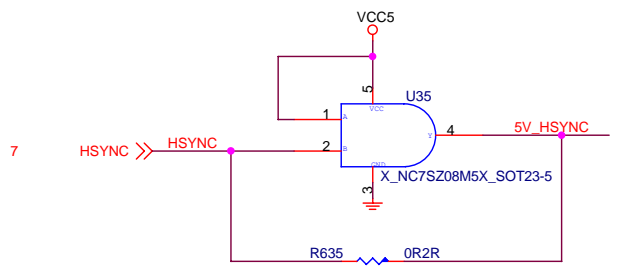
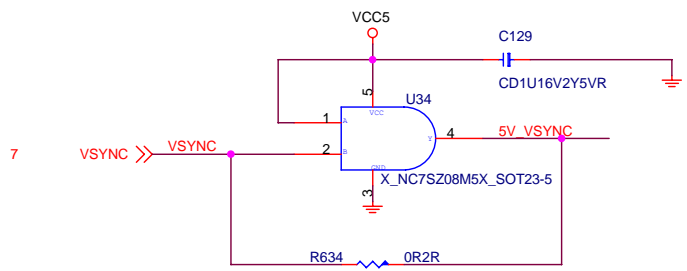
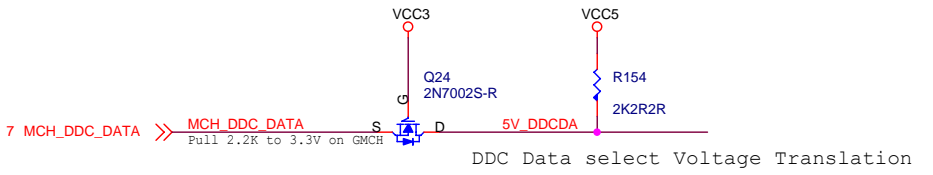
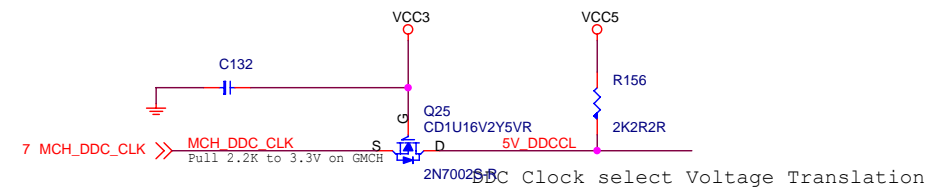


Link to the Future

MICRO-START INT'L CO.,LTD.

Title		
IEEE-1394 VIA-VT6308		
Size	Document Number	Rev
Custpm	MS-7356	0B
Date:	Monday, February 26, 2007	Sheet 21 of 36





VCC3	3,4,7,9,11,12,13,14,15,16,17,18,19,20,21,22,23,27,28,30
VCC5	15,16,18,19,20,22,23,26,27,28,29,30
PGND	25,26
AGND	22,30
GND	3,4,5,6,7,8,9,10,11,12,13,14,15,16,17,18,19,20,21,22,23,25,26,27,28,29,30

MICRO-START INT'L CO.,LTD.

Title

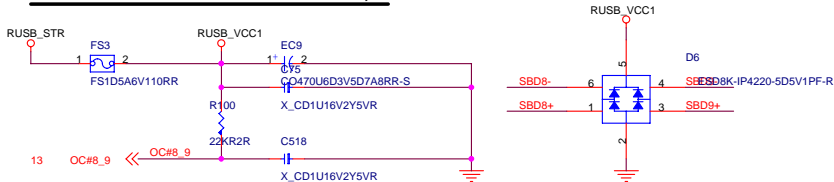
On Board VGA Connector

Size	Document Number	Rev
Custom	MS-7356	0B

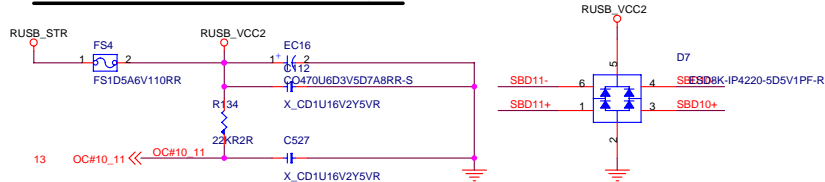
Date: Monday, February 26, 2007 Sheet 24 of 36

Rear USB Connector

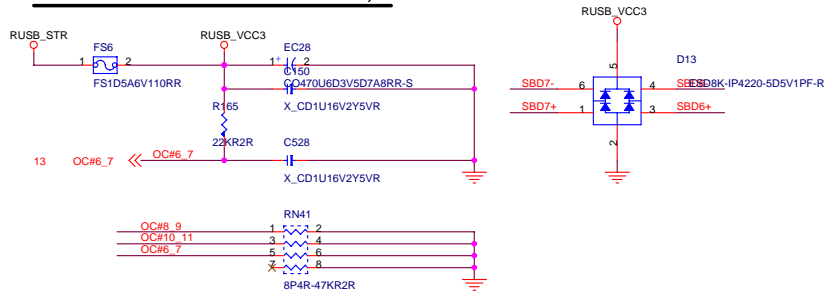
POWER CIRCUIT FOR USB PORT 3,6



POWER CIRCUIT FOR USB PORT 9,10

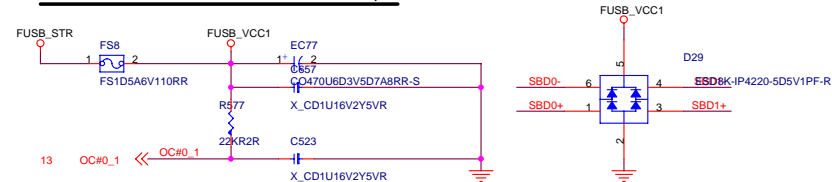


POWER CIRCUIT FOR USB PORT 0,2

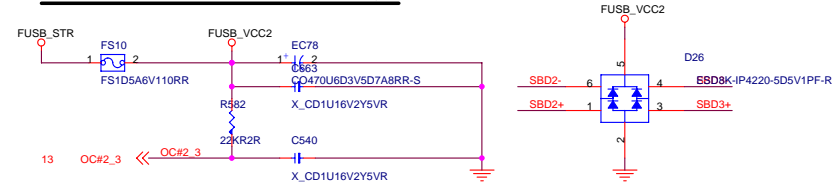


Front USB Connector

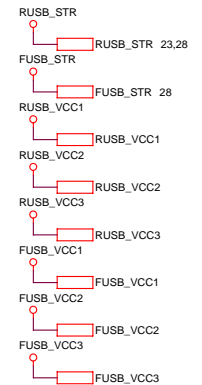
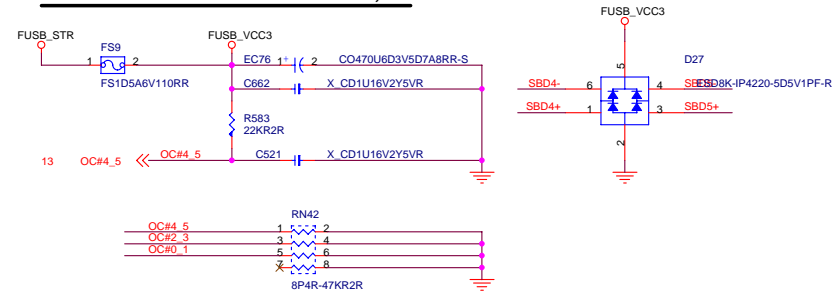
POWER CIRCUIT FOR USB PORT 1,4



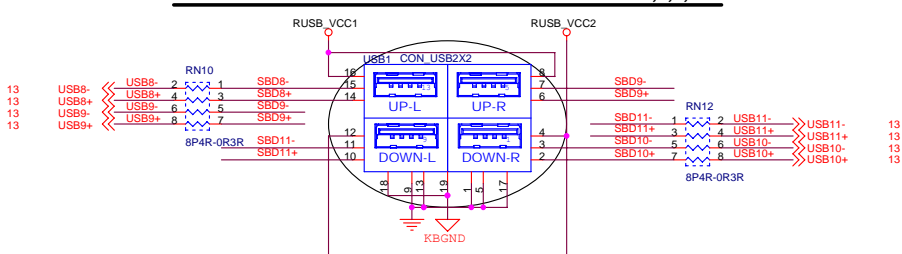
POWER CIRCUIT FOR USB PORT 5,7



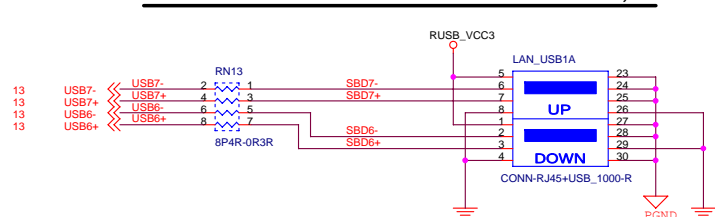
POWER CIRCUIT FOR USB PORT 8,11



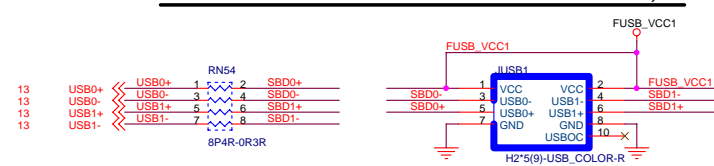
REAR PANEL USB CONNECTOR FOR USB PORT 6,3,9,10



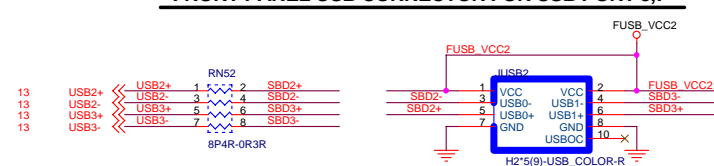
REAR PANEL USB CONNECTOR FOR USB PORT 0,2



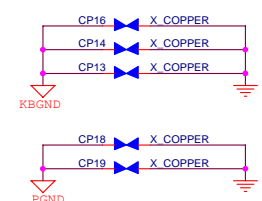
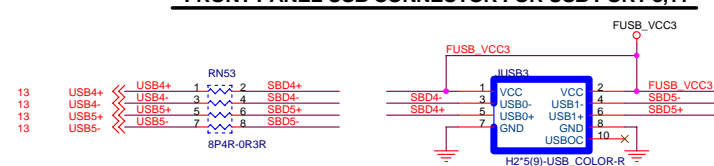
FRONT PANEL USB CONNECTOR FOR USB PORT 1,4

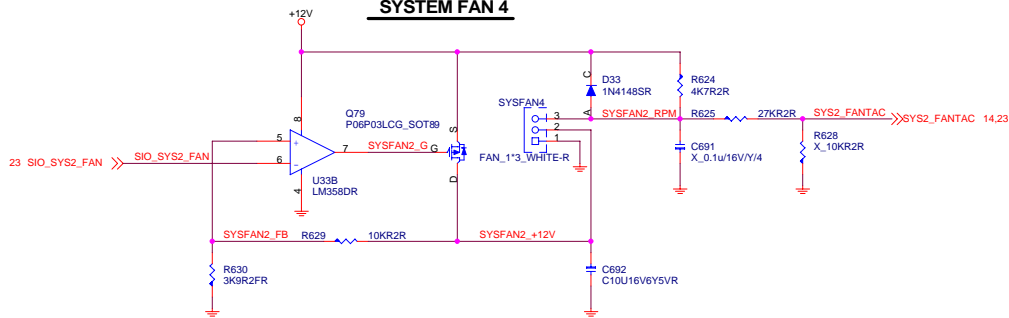
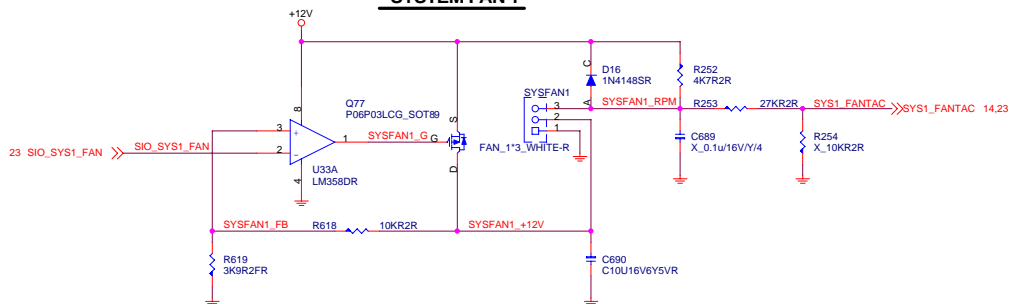
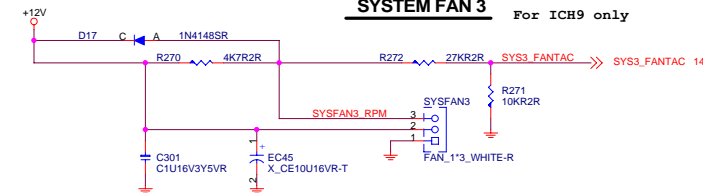
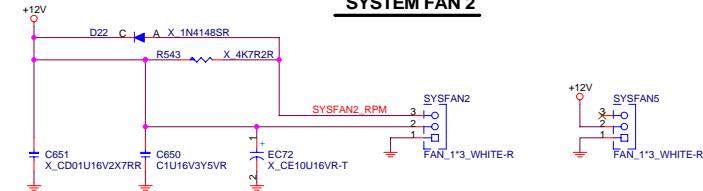
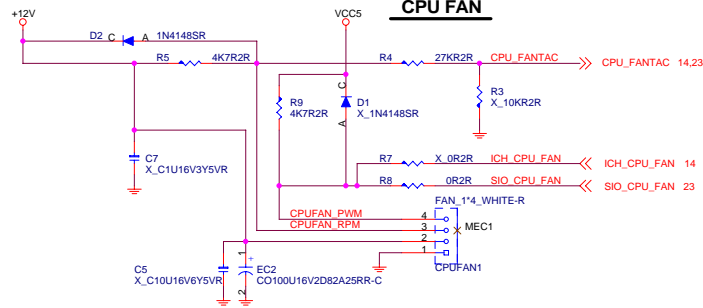


FRONT PANEL USB CONNECTOR FOR USB PORT 5,7



FRONT PANEL USB CONNECTOR FOR USB PORT 8,11

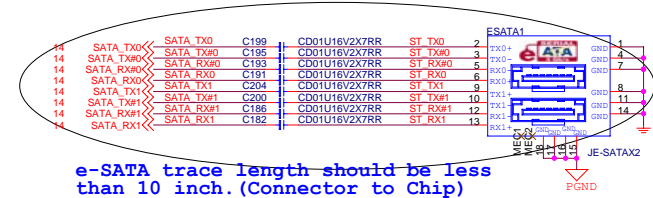


[illegible]

Pin connection diagram for RN17:

- Pin 1: SYS2_FANTAC
- Pin 2: CPU_FANTAC
- Pin 3: SYST_FANTAC
- Pin 4: Common Ground
- Pin 5: Common Ground
- Pin 6: Common Ground
- Pin 7: Common Ground
- Pin 8: Unconnected

Component: RN17, 8P4R-10KR2R



C374 CD1U16V2Y5VR
 C383 CD1U16V2Y5VR
 C387 CD1U16V2Y5VR
 5VSB
 R275 10R2R
 R600 11K2RFR
 C362 C1U16V3X5SR
 1.8VREF
 REF_PWR
 U14
 5VSB
 1.8V
 7 1.8VREF
 3 SCL
 22R2R
 SMBCLK_REF
 3 SMBCLK_ISO
 11.27,30 SMBCLK_ISO
 4 SDA
 22R2R
 SMBDATA_REF
 4 SMBDATA_ISO
 11.27,30 SMBDATA_ISO
 29 5VDRV1
 5VDRV1
 R287 200K2RFR
 REF_ENB
 8 EN
 GND
 2
 R298 56K2RFR
 1.2V
 5 1.2VREF
 1.25VREF
 6 1.25VREF
 UPE261
 *5VSB > 4.2V POR
 *Pin8 > 1.0V Enable
 *Pin8 < 0.4V Disable
 DDR_REF
 NB 1.25V REF
 V_FSB_VTT REF
 *Reference sinking/sourcing 100uA
 *Reference ramp-up 5mS

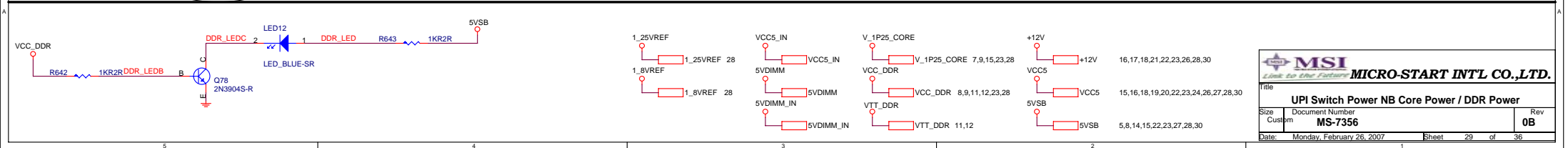
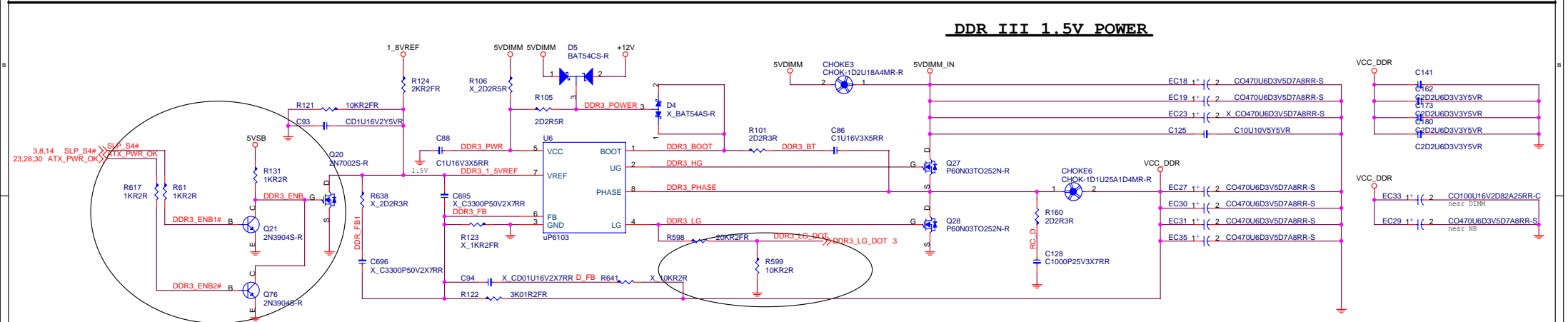
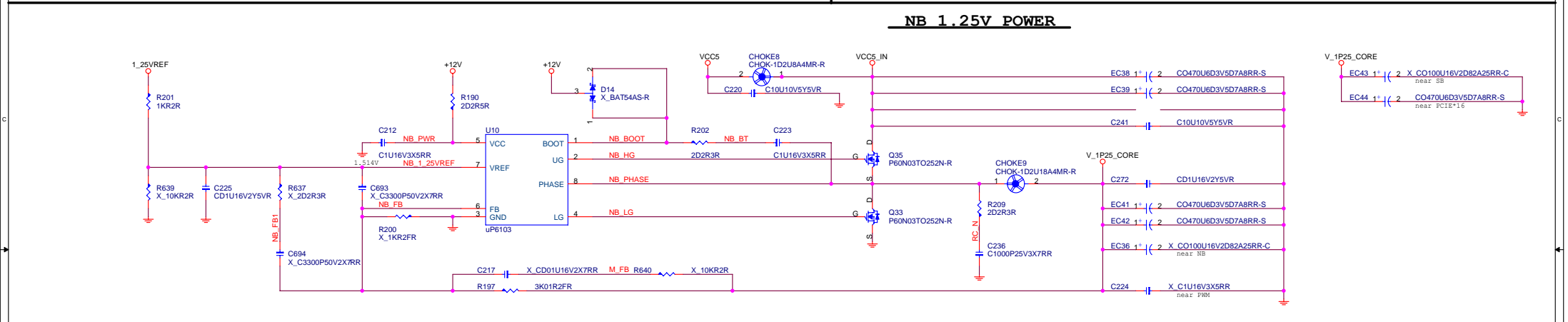
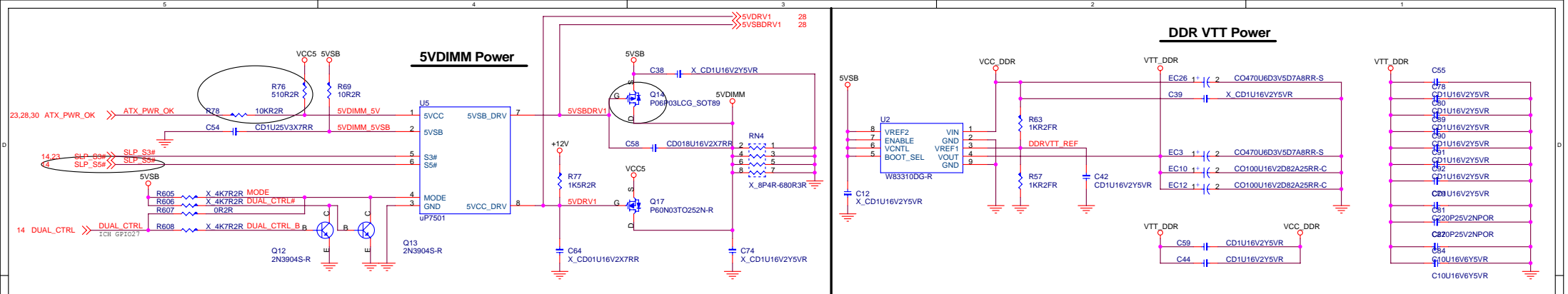
The circuit diagram shows a 1.5V voltage divider using a U16C LM324M-R op-amp configured as a voltage follower. The non-inverting input (+) is connected to a divider of VCC1_5REF (1.5V) and VCC3 (3.3V) via resistors R325 (10K) and R329 (150K). The output (pin 1) is connected to the inverting input (-) via a feedback resistor R426 (10K) and to the ICH pin of the IC50 COB20U2D5V6D1A7RR-S via a resistor R315 (4K7) and a capacitor C426. The op-amp is powered by VCC3 (3.3V) and has its ground connected to the common ground. A 1.5V ICH pin connection table is provided below the circuit.

ICH GPIO2/3 for over voltage V_1P5_ICH		
V1_5SET_0=0	V1_5SET_1=0	1.5V
V1_5SET_0=1	V1_5SET_1=0	1.6V
V1_5SET_0=0	V1_5SET_1=1	1.7V
V1_5SET_0=1	V1_5SET_1=1	1.8V

[illegible]

PWROK DELAY

The diagram illustrates the PWROK delay circuit. It consists of three main signal paths, each involving a transistor (Q55, Q34, Q75) and a resistor network. The inputs are VCC3, ICH_VRM_PGD, and ATX_PWR_OK. The outputs are CHIP_PWGD_B, VRM_PWRGD_B, and ATX_PWR_OK_B. The circuit is designed to delay the PWROK signal until the power is stable.



[illegible]

H.D. LED

20 JM_IDELED# << JM_IDELED#

14 ICH_SATALED# << ICH_SATALED#

Open-collector

Q21 BAT54AS-R

3

HDDL

C846 X_CD1U16V25Y5R

The schematic diagram illustrates the front panel connections for the J1939-ECU. It features two connector blocks, JFP1 (Front Panel A-R) and JFP2 (Front Panel B-R). JFP1 has pins 1-9 connected to various signals: 1 to HDD+, 2 to PLED, 3 to HDDLED, 4 to SLED, 5 to RESET, 6 to PWSW+, 7 to RESE+, 8 to PWSW-, and 9 to NC. JFP2 has pins 1-8 connected to: 1 to GND, 2 to BUZZER-, 3 to SLED, 4 to BUZ+, 5 to PLED, 6 to BUZ-, 7 to VCCSPK, and 8 to VCCS. The diagram also shows the internal wiring of the ECU, including resistors (R527, R534, R539, R536), capacitors (C623, C647, C619), and LEDs (LED5, LED4, LED3, LED2). The test harness is connected to the ECU via a 3VSB supply and various signal lines (WDT#, WDT#, FP_RST#, R_FP_RST#, SWITCH_ON#, PWRBTN, PWR_LED, HDD+, SLED, PLED, BUZZER-, BUZ+, BUZ-, VCCSPK, VCCS).

[illegible]